**APPLIED MICRO CIRCUITS CORPORATION**

# PPC460EX

| | *Application Note* |
|---|---|

## Interface Guide

This document lists the PPC460EX signals by interface and identifies register settings needed to configure shared signals. It is intended to complement the alphabetical signal listing in the data sheet and the register descriptions in the user's manual.

### Shared I/O

The PPC460EX has several I/O which are shared between internal controllers and require configuration by initialization software to enable. The matrix in *Figure 1* identifies the interfaces affected by shared I/O. Intersecting rows and columns with shaded cells indicate two interfaces with common I/O. Depending on the interfaces, the shared I/O can either restrict the function of the interfaces if both possible signal functions are needed or eliminate the possibility of using one of the interfaces. To resolve the effect of shared I/O on a particular interface review the signals for each interface.

In addition to the shared interfaces in *Figure 1*, many signals are also shared internally with GPIO. Signals shared with GPIO are by default configured as GPIO receivers after reset. Software must configure GPIO registers to select the desired function of shared GPIO signals. The GPIO register configurations are included in this document. See *Table 16* and *Table 17* for a list of GPIO signals.

GPIO register bit fields are identified by square brackets. For example, bit field 20:21 of GPIO0_ISR2H is documented as GPIO0_ISR2H[20:21].

Figure 1. Shared I/O Matrix

| | DMA Channel0 | DMA Channel1 | DMA Channel2 | DMA Channel3 | EBC PerAddr05:07 | EBC PerCS0:5 | EBC PerPar0:3 | NAND NFC0:3 | IRQ04:15 | IIC1 | PCIE0 (1 lane) | SATA | SPI | UART0 8-pin | UART0 4-pin | UART1 4-pin | UART1 2-pin | UART2 2-pin | UART3 2-pin |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DMA Channel0 | | | | | ■ | | | | ■ | | | | | | | | | | |
| DMA Channel1 | | | | | | ■ | | | ■ | | | | | | | | | | |
| DMA Channel2 | | | | | | | ■ | | ■ | | | | | | | | | | |
| DMA Channel3 | | | | | | | ■ | ■ | ■ | | | | ■ | ■ | | | | | ■ |
| PerAddr05:07 | ■ | | | | | | | | ■ | | | | | | | | | | |
| EBC PerCS0:5 | | ■ | | | | | ■ | | ■ | | | | | | | | | | |
| EBC PerPar0:3 | | | ■ | ■ | | ■ | | ■ | ■ | | | | | | | | | | |
| NAND NFC0:3 | | | | ■ | | | ■ | | ■ | | | | | ■ | | ■ | ■ | ■ | |
| IRQ04:15 | ■ | ■ | ■ | ■ | ■ | ■ | ■ | ■ | | | | | | ■ | | ■ | ■ | | |
| IIC1 | | | | | | | | | | | ■ | | | | | | | | |
| PCIE0 (1 lane) | | | | | | | | | | ■ | | | | | | | | | |
| SATA | | | | | | | | | | | | | ■ | | | | | | |
| SPI | | | | ■ | | | | | | | | ■ | | | ■ | | | ■ | |
| UART0 8-pin | | | | ■ | | | | ■ | ■ | | | | | | ■ | ■ | ■ | ■ | ■ |
| UART0 4-pin | | | | | | | | | | | | | ■ | ■ | | ■ | | | ■ |
| UART1 4-pin | | | | | | | | ■ | ■ | | | | | ■ | ■ | | ■ | | |
| UART1 2-pin | | | | | | | | ■ | ■ | | | | | ■ | | ■ | | | |
| UART2 2-pin | | | | | | | | ■ | | | | | ■ | ■ | | | | | |
| UART3 2-pin | | | | ■ | | | | | | | | | | ■ | ■ | | | | |

## Ethernet

The PPC460EX supports three types of Ethernet interfaces (SGMII, GMII, MII and RGMII). Table 1 lists the Ethernet interface combinations supported by EMAC0 and EMAC1. *Table 2 - Table 4* describe how to configure each Ethernet interface. See *Table 12 - Table 15* for the Ethernet signals.

*Table 1. Shared Ethernet Interfaces*

| Configuration | EMAC0 (QoS, TAH)* | EMAC1 (QoS, TAH)* |
|:---:|:---:|:---:|
| 1 | RGMII0 | RGMII1 |
| 2 | RGMII0 | SGMII1 |
| 3 | GMII0 or MII0 | SGMII1 |
| 4 | SGMII0 | SGMII1 |

*EMAC0 and EMAC1 have QoS and TAH support.
QoS - Quality of Service
TAH - TCP/IP Accelerator Hardware

Note: TAH logic is selected by:
SDR0_ETH_CFG[TAHOE0_BYPASS]
SDR0_ETH_CFG[TAHOE1_BYPASS]

*Table 2. MII/GMII Configuration*

| MII/ GMII Interface | Configuration |
|:---:|:---|
| MII0 | MII through the ZMII bridge:<br>EMAC0<>ZMII Bridge 0 <>MII0<br><br>When using the ZMII bridge, GMCRefClk is not required.<br><br>SDR0_ETH_CFG[SGMII0_LPBK]=0<br>SDR0_ETH_CFG[SGMII0_ENABLE]=0<br>SDR0_ETH_CFG[ZMIM]=0b00<br>SDR0_ETH_CFG[GMC0BS]=1<br>ZMII0_FER[MII0]=1<br>EMAC0_MR1[MF]=0b00 for 10Mbit<br>EMAC0_MR1[MF]=0b01 for 100Mbit |

*Table 2. MII/GMII Configuration*

| MII/ GMII Interface | Configuration |
|---|---|
| GMII0/MII0 | GMII/MII through the RGMII bridge: EMAC0<>RGMII Bridge 0 <>GMII0/MII0<br><br>GMCRefClk is required.<br><br>SDR0_ETH_CFG[SGMII0_LPBK]=0<br>SDR0_ETH_CFG[SGMII0_ENABLE]=0<br>SDR0_ETH_CFG[GMC0BS]=0<br>RGMII0_FER[CH0CFG]=0b111<br>RGMII0_FER[CH1CFG]=0b011<br>EMAC0_MR1[MF]=0b00 for 10Mbit<br>EMAC0_MR1[MF]=0b01 for 100Mbit<br>EMAC0_MR1[MF]=0b10 for 1000Mbit<br>RGMII0_SSR[SP0] ignored |

*Table 3. RGMII Configuration*

| RGMII Interface | Configuration |
|---|---|
| RGMII0 | EMAC0<>RGMII Bridge 0<>RGMII0<br><br>SDR0_ETH_CFG[SGMII0_LPBK]=0<br>SDR0_ETH_CFG[SGMII0_ENABLE]=0<br>SDR0_ETH_CFG[GMC0BS]=0<br>RGMII0_FER[CH0CFG]=0b101<br>RGMII0_FER[CH1CFG]=0b101<br>Set EMAC0_MR1[MF]=0b10 for RGMII.<br>Enables GMII between the EMAC and RGMII bridge.<br>Set RGMII0_SSR[SP0] for line speed. |
| RGMII1 | EMAC1<>RGMII Bridge 0<>RGMII1<br><br>SDR0_ETH_CFG[SGMII1_LPBK]=0<br>SDR0_ETH_CFG[SGMII1_ENABLE]=0<br>SDR0_ETH_CFG[GMC0BS]=0<br>RGMII0_FER[CH0CFG]=0b101<br>RGMII0_FER[CH1CFG]=0b101<br>Set EMAC1_MR1[MF]=0b10 for RGMII.<br>Enables GMII between the EMAC and RGMII bridge.<br>Set RGMII0_SSR[SP1] for line speed. |

*Table 4. SGMII Configuration*

| SGMII Interface | Configuration |
|---|---|
| SGMII0 | EMAC0<>GPSC0 <>SGMII SerDes 0<br><br>SDR0_ETH_CFG[SGMII0_LPBK]=0<br>SDR0_ETH_CFG[SGMII0_ENABLE]=1<br><br>Set EMAC0_MR1[MF]=0b11.<br>Enables TBI between the EMAC and internal SGMII SerDes. |
| SGMII1 | EMAC1<>GPSC1 <>SGMII SerDes 1<br><br>SDR0_ETH_CFG[SGMII1_LPBK]=0<br>SDR0_ETH_CFG[SGMII1_ENABLE]=1<br><br>Set EMAC1_MR1[MF]=0b11.<br>Enables TBI between the EMAC and internal SGMII SerDes. |

EMAC Gigabit mode Physcial Coding Sublayer (GPSC) registers must be configured when using SGMII mode. The internal communication between the EMAC and SGMII SerDes is ten bit mode (TBI).

# UART

The PPC460EX has four UART controllers with 8 shared pins. *Table 5* lists the UART interface combinations supported using these shared pins. *Table 6* describes how to configure each UART interface. See *Table 28 - 32* for the UART signals.

*Table 5. Shared UART Interfaces*

| Configuration | UART0 | UART1 | UART2 | UART3 |
|:---:|:---:|:---:|:---:|:---:|
| 1 | 8-pin | | | |
| 2 | 4-pin | 4-pin | | |
| 3 | 4-pin | 2-pin | 2-pin | |
| 4 | 2-pin | 2-pin | 2-pin | 2-pin |

*Table 6. UART Interface Configuration*

| Configuration | Configuration |
|:---:|:---|
| 1 | Configuration for UART0 8-pin mode:<br>Set SDR0_PFC1[U0IM]=0 for UART0 in 8 bit mode.<br>Set UART0_MCR[AFC]=1 to enable flow control.<br>Configure GPIO controller. See Table 28. |
| 2 | Configuration for UART0 4-pin mode and UART1 4-pin mode:<br>Set SDR0_PFC1[U0IM]=1<br>Set SDR0_PFC1[U0ME]=1<br>Set SDR0_PFC1[U1ME]=1<br>Set UART0_MCR[AFC]=1 to enable flow control.<br>Set UART1_MCR[AFC]=1 to enable flow control.<br>Configure GPIO controller. See Table 29. |
| 3 | Configuration for UART0 4-pin mode, UART1 2-pin mode and UART2 2-pin mode:<br>Set SDR0_PFC1[U0IM]=1<br>SDR0_PFC1[U0ME]=1<br>Set UART0_MCR[AFC]=1 to enable flow control.<br>Set UART1_MCR[AFC]=0 to disable flow control.<br>Set UART2_MCR[AFC]=0 to disable flow control.<br>Configure GPIO controller. See Table 30. |
| 4 | Configuration for UART0 2-pin mode, UART1 2-pin mode, UART2 2-pin mode and UART3 2-pin mode:<br>Set UART0_MCR[AFC]=0 to disable flow control.<br>Set UART1_MCR[AFC]=0 to disable flow control.<br>Set UART2_MCR[AFC]=0 to disable flow control.<br>Set UART3_MCR[AFC]=0 to disable flow control.<br>Configure GPIO controller. See Table 31. |

*Application Note*

## Signal List

Table 7 through Table 34 list the signals by interface. Where I/O are shared, register configurations are included in the configuration column. Configurations that affect the entire interface are listed as table footnotes.

*Table 7. DDR Interface*

| PPC460EX Signals | Ball | DDR | I/O | Configuration |
|---|---|---|---|---|
| MemData00 | P30 | MemData00 | | |
| MemData01 | N34 | MemData01 | | |
| MemData02 | R32 | MemData02 | | |
| MemData03 | R30 | MemData03 | | |
| MemData04 | N33 | MemData04 | | |
| MemData05 | N32 | MemData05 | | |
| MemData06 | P34 | MemData06 | | |
| MemData07 | R31 | MemData07 | | |
| MemData08 | R34 | MemData08 | | |
| MemData09 | T34 | MemData09 | | |
| MemData10 | V34 | MemData10 | | |
| MemData11 | T32 | MemData11 | | |
| MemData12 | R33 | MemData12 | | MemData00 -MSb |
| MemData13 | T31 | MemData13 | | MemData63 - LSb |
| MemData14 | U33 | MemData14 | | |
| MemData15 | U34 | MemData15 | | Connect MemData00:31 for a 32-bit interface. |
| MemData16 | V32 | MemData16 | I/O | Connect MemData00:63 for a 64-bit interface. |
| MemData17 | V31 | MemData17 | | |
| MemData18 | Y32 | MemData18 | | Unused signals do not require termination. |
| MemData19 | W30 | MemData19 | | |
| MemData20 | V33 | MemData20 | | |
| MemData21 | W34 | MemData21 | | |
| MemData22 | Y34 | MemData22 | | |
| MemData23 | Y33 | MemData23 | | |
| MemData24 | AA33 | MemData24 | | |
| MemData25 | AA32 | MemData25 | | |
| MemData26 | AB31 | MemData26 | | |
| MemData27 | Y30 | MemData27 | | |
| MemData28 | AA34 | MemData28 | | |
| MemData29 | Y31 | MemData29 | | |
| MemData30 | AB33 | MemData30 | | |
| MemData31 | AB32 | MemData31 | | |

*Table 7. DDR Interface*

| PPC460EX Signals | Ball | DDR | I/O | Configuration |
|---|---|---|---|---|
| MemData32 | AM26 | MemData32 | | |
| MemData33 | AP26 | MemData33 | | |
| MemData34 | AK21 | MemData34 | | |
| MemData35 | AN24 | MemData35 | | |
| MemData36 | AL26 | MemData36 | | |
| MemData37 | AK26 | MemData37 | | |
| MemData38 | AL24 | MemData38 | | |
| MemData39 | AM24 | MemData39 | | |
| MemData40 | AL23 | MemData40 | | |
| MemData41 | AM23 | MemData41 | | |
| MemData42 | AM21 | MemData42 | | |
| MemData43 | AN21 | MemData43 | | |
| MemData44 | AK23 | MemData44 | | |
| MemData45 | AP24 | MemData45 | | |
| MemData46 | AP22 | MemData46 | | |
| MemData47 | AL21 | MemData47 | I/O | Unused signals do not require termination. |
| MemData48 | AL20 | MemData48 | | |
| MemData49 | AM20 | MemData49 | | |
| MemData50 | AL18 | MemData50 | | |
| MemData51 | AM18 | MemData51 | | |
| MemData52 | AK20 | MemData52 | | |
| MemData53 | AP21 | MemData53 | | |
| MemData54 | AP20 | MemData54 | | |
| MemData55 | AP19 | MemData55 | | |
| MemData56 | AP18 | MemData56 | | |
| MemData57 | AN17 | MemData57 | | |
| MemData58 | AL16 | MemData58 | | |
| MemData59 | AP15 | MemData59 | | |
| MemData60 | AK18 | MemData60 | | |
| MemData61 | AN18 | MemData61 | | |
| MemData62 | AM16 | MemData62 | | |
| MemData63 | AK16 | MemData63 | | |
| MemAddr00 | AK34 | MemAddr00 | | |
| MemAddr01 | AJ33 | MemAddr01 | | MemAddr14 - MSb |
| MemAddr02 | AJ32 | MemAddr02 | | MemAddr00 - LSb |
| MemAddr03 | AJ34 | MemAddr03 | | |
| MemAddr04 | AH30 | MemAddr04 | | The DDR address signals must be connected to |
| MemAddr05 | AH31 | MemAddr05 | | the DDR memory as follows: |
| MemAddr06 | AH32 | MemAddr06 | | |
| MemAddr07 | AG31 | MemAddr07 | O | MemAddr14 - DDR A14 |
| MemAddr08 | AH34 | MemAddr08 | | MemAddr13 - DDR A13 |
| MemAddr09 | AG32 | MemAddr09 | | MemAddr12 - DDR A12 |
| MemAddr10 | AG33 | MemAddr10 | | . |
| MemAddr11 | AF31 | MemAddr11 | | . |
| MemAddr12 | AG34 | MemAddr12 | | . |
| MemAddr13 | AC29 | MemAddr13 | | MemAddr00 - DDR A00 |
| MemAddr14 | AF32 | MemAddr14 | | |

*Table 7. DDR Interface*

| PPC460EX Signals | Ball | DDR | I/O | Configuration |
|---|---|---|---|---|
| ECC0<br>ECC1<br>ECC2<br>ECC3<br>ECC4<br>ECC5<br>ECC6<br>ECC7 | AC31<br>AC30<br>AE32<br>AE34<br>AC34<br>AC32<br>AD31<br>AD30 | ECC0<br>ECC1<br>ECC2<br>ECC3<br>ECC4<br>ECC5<br>ECC6<br>ECC7 | I/O | ECC0 - MSb<br>ECC7 - LSb<br><br>Connect ECC0:7 for a 32-bit or 64-bit interface.<br><br>ECC memory must support the same address mode as the data memory. If unsure about the address mode, use the same memory type for ECC and data.<br><br>Unused signals do not require termination. |
| DQS0<br>DQS1<br>DQS2<br>DQS3<br>DQS4<br>DQS5<br>DQS6<br>DQS7<br>DQS8 | P33<br>U32<br>W31<br>AA30<br>AP25<br>AN22<br>AM19<br>AK17<br>AD32 | DQS0<br>DQS1<br>DQS2<br>DQS3<br>DQS4<br>DQS5<br>DQS6<br>DQS7<br>DQS8 | I/O | DQS0/$\overline{DQS0}$ - Strobe for MemData00:07<br>DQS1/$\overline{DQS1}$ - Strobe for MemData08:15<br>DQS2/$\overline{DQS2}$ - Strobe for MemData16:23<br>DQS3/$\overline{DQS3}$ - Strobe for MemData24:31<br>DQS4/$\overline{DQS4}$ - Strobe for MemData32:39<br>DQS5/$\overline{DQS5}$ - Strobe for MemData40:47<br>DQS6/$\overline{DQS6}$ - Strobe for MemData48:55<br>DQS7/$\overline{DQS7}$ - Strobe for MemData56:63<br>DQS8/$\overline{DQS8}$ - Strobe for ECC0:7<br><br>Unused signals do not require termination. |
| $\overline{DQS0}$<br>$\overline{DQS1}$<br>$\overline{DQS2}$<br>$\overline{DQS3}$<br>$\overline{DQS4}$<br>$\overline{DQS5}$<br>$\overline{DQS6}$<br>$\overline{DQS7}$<br>$\overline{DQS8}$ | P32<br>U31<br>W32<br>AA31<br>AN25<br>AM22<br>AL19<br>AL17<br>AD33 | $\overline{DQS0}$<br>$\overline{DQS1}$<br>$\overline{DQS2}$<br>$\overline{DQS3}$<br>$\overline{DQS4}$<br>$\overline{DQS5}$<br>$\overline{DQS6}$<br>$\overline{DQS7}$<br>$\overline{DQS8}$ | I/O | |
| DM0<br>DM1<br>DM2<br>DM3<br>DM4<br>DM5<br>DM6<br>DM7<br>DM8 | P31<br>U30<br>V30<br>AB34<br>AM25<br>AP23<br>AN20<br>AM17<br>AD34 | DM0<br>DM1<br>DM2<br>DM3<br>DM4<br>DM5<br>DM6<br>DM7<br>DM8 | I/O | DM0 - Mask for MemData00:07<br>DM1 - Mask for MemData08:15<br>DM2 - Mask for MemData16:23<br>DM3 - Mask for MemData24:31<br>DM4 - Mask for MemData32:39<br>DM5 - Mask for MemData40:47<br>DM6 - Mask for MemData48:55<br>DM7 - Mask for MemData56:63<br>DM8 - Mask for ECC0:7<br><br>Unused signals do not require termination. |
| BA0<br>BA1<br>BA2 | AN32<br>AP31<br>AM31 | BA0<br>BA1<br>BA2 | O | |
| MemDCFdbkD | AM33 | MemDCFdbkD | O | Connect feedback MemDCFdbkD directly to MemDCFdbkR. The shortest trace should be used. |
| MemDCFdbkR | AM34 | MemDCFdbkR | I | |

*Application Note*

*Table 7. DDR Interface*

| PPC460EX Signals | Ball | DDR | I/O | Configuration |
|---|---|---|---|---|
| MemODT0<br>MemODT1<br>MemODT2<br>MemODT3 | AP28<br>AM27<br>AM28<br>AL27 | MemODT0<br>MemODT1<br>MemODT2<br>MemODT3 | O | Only used for DDR2.<br><br>MemODT0 - ODT for Rank 0<br>MemODT1 - ODT for Rank 1<br>MemODT2 - ODT for Rank 2<br>MemODT3 - ODT for Rank 3<br><br>Unused signals do not require termination. |
| ClkEn0<br>ClkEn1<br>ClkEn2<br>ClkEn3 | AE29<br>AF34<br>AE33<br>AE31 | ClkEn0<br>ClkEn1<br>ClkEn2<br>ClkEn3 | O | ClkEn0 - clock enable for Rank 0<br>ClkEn1 - clock enable for Rank 1<br>ClkEn2 - clock enable for Rank 2<br>ClkEn3 - clock enable for Rank 3 |
| MemClkOut0<br>$\overline{\text{MemClkOut0}}$ | AP27<br>AN27 | MemClkOut0<br>$\overline{\text{MemClkOut0}}$ | O | Duplicate output clocks. |
| MemClkOut1<br>$\overline{\text{MemClkOut1}}$ | AK31<br>AK32 | MemClkOut1<br>$\overline{\text{MemClkOut1}}$ | O | |
| $\overline{\text{BankSel0}}$<br>$\overline{\text{BankSel1}}$<br>$\overline{\text{BankSel2}}$<br>BankSel3 | AL28<br>AP29<br>AM29<br>AN29 | $\overline{\text{BankSel0}}$<br>$\overline{\text{BankSel1}}$<br>$\overline{\text{BankSel2}}$<br>BankSel3 | O | $\overline{\text{BankSel0}}$ - Chip select for Rank 0<br>$\overline{\text{BankSel1}}$ - Chip select for Rank 1<br>$\overline{\text{BankSel2}}$ - Chip select for Rank 2<br>BankSel3 - Chip select for Rank 3 |
| $\overline{\text{RAS}}$ | AP30 | $\overline{\text{RAS}}$ | O | |
| $\overline{\text{CAS}}$ | AL29 | $\overline{\text{CAS}}$ | O | |
| $\overline{\text{WE}}$ | AP32 | $\overline{\text{WE}}$ | O | |
| MemVRef1A<br>MemVRef1B<br>MemVRef2A<br>MemVRef2B | AJ19<br>AB29<br>AJ22<br>T29 | MemVRef1A<br>MemVRef1B<br>MemVRef2A<br>MemVRef2B | na | Duplicate reference voltage analog inputs.<br>Connect to the same reference. |

*Table 8. Debug - Instruction Trace Interface*

| PPC460EX Signals | Ball | Trace | I/O | Configuration |
|---|---|---|---|---|
| TrcClk | M29 | TrcClk | O | Output clock frequency: CPU Clk/4 |
| [TrcBS0]GPIO49 | H33 | TrcBS0/ | O | SDR0_PFC0[DBG]=1<br>CCR0[DTB]=0 |
| [TrcBS1]GPIO50 | J34 | TrcBS1/TrcBR1 | O | |
| [TrcBS2]GPIO51 | H34 | TrcBS2/TrcBR1 | O | |
| [TrcES0]GPIO52 | L30 | TrcES0TrcBR1 | O | |
| [TrcES1]GPIO53 | L31 | TrcES1 | O | |
| [TrcES2]GPIO54 | K33 | TrcES2 | O | |
| [TrcES3]GPIO55 | L32 | TrcES3 | O | |
| [TrcES4]GPIO56 | K34 | TrcES4 | O | |
| [TrcTS0]GPIO57 | L33 | TrcTS0 | O | |
| [TrcTS1]GPIO58 | N29 | TrcTS1 | O | |
| [TrcTS2]GPIO59 | M31 | TrcTS2 | O | |
| [TrcTS3]GPIO60 | L34 | TrcTS3 | O | |
| [TrcTS4]GPIO61 | M32 | TrcTS4 | O | |
| [TrcTS5]GPIO62 | M34 | TrcTS5 | O | |
| [TrcTS6]GPIO63 | N31 | TrcTS6 | O | |

*Table 9. Debug - JTAG Interface*

| PPC460EX Signals | Ball | JTAG | I/O | Configuration |
|---|---|---|---|---|
| TCK | J29 | TCK | I | Pull-up required |
| TDI | F34 | TDI | I | Has internal pull-up. |
| TDO | F33 | TDO | O | |
| TMS | G32 | TMS | I | Has internal pull-up. |
| $\overline{TRST}$ | H29 | $\overline{TRST}$ | I | Has internal pull-up.<br>Must be driven low during a power-on reset. |
| $\overline{HALT}$ | H32 | $\overline{HALT}$ | I | Has internal pull-up. |

*Application Note*

*Table 10. DMA Controller (DMA2P40) Interface*

| PPC460EX Signals | Ball | DMA2P40 | I/O | Configuration |
|---|---|---|---|---|
| *DMA Channel 0* | | | | |
| [DMAAck0]GPIO47[PerAddr06][IRQ14] | C31 | DMAAck0 | O | GPIO1_OSRL[30:31]=0b10<br>GPIO1_TSRL[30:31]=0b10 |
| [DMAReq0]GPIO46[PerAddr05][IRQ13] | B32 | DMAReq0 | I | GPIO1_TSRL[28:29]=0b10<br>GPIO1_ISR2L[28:29]=0b01 |
| [EOT0/TC0]GPIO48[PerAddr07][IRQ15] | D30 | EOT0/TC0 | I/O | GPIO1_OSRH[0:1]=0b10<br>GPIO1_TSRH[0:1]=0b10<br>GPIO1_ISR2H[0:1]=0b01<br><br>To enable EOT, set DMA2P40_CR0[ETD]=0. EOT is an input.<br><br>To enable TC, set DMA2P40_CR0[ETD]=1. TC is an output. |
| *DMA Channel 1* | | | | |
| [DMAAck1]GPIO44[PerCS4][IRQ11] | E21 | DMAAck1 | O | GPIO1_OSRL[24:25]=0b10<br>GPIO1_TSRL[24:25]=0b10 |
| [DMAReq1]GPIO43[PerCS3][NFCE3][IRQ10] | A22 | DMAReq1 | I | GPIO1_TSRL[22:23]=0b10<br>GPIO1_ISR2L[22:23]=0b01 |
| [EOT1/TC1]GPIO45[PerCS5][IRQ12] | D21 | EOT1/TC1 | I/O | GPIO1_OSRL[26:27]=0b10<br>GPIO1_TSRL[26:27]=0b10<br>GPIO1_ISR1L[26:27]=0b01<br><br>To enable EOT, set DMA2P40_CR1[ETD]=0. EOT is an input.<br><br>To enable TC, set DMA2P40_CR1[ETD]=1. TC is an output. |
| *DMA Channel 2* | | | | |
| [DMAAck2]GPIO31[PerPar1][IRQ8] | A16 | DMAAck2 | O | GPIO0_OSRH[30:31]=0b10<br>GPIO0_TSRH[30:31]=0b10 |
| [DMAReq2]GPIO30[PerPar0][IRQ7] | A20 | DMAReq2 | I | GPIO0_TSRH[28:29]=0b10<br>GPIO0_ISR2H[28:29]=0b01 |
| [EOT2/TC2]GPIO32[PerPar2][IRQ9] | A14 | EOT2/TC2 | I/O | GPIO1_OSRL[0:1]=0b10<br>GPIO1_TSRL[0:1]=0b10<br>GPIO1_ISR2L[0:1]=0b01<br><br>To enable EOT, set DMA2P40_CR2[ETD]=0. EOT is an input.<br><br>To enable TC, set DMA2P40_CR2[ETD]=1. TC is an output. |
| *DMA Channel 3* | | | | |
| [DMAAck3]GPIO36[UART0CTS][UART3Rx] | E31 | DMAAck3 | O | GPIO1_OSRL[8:9]=0b10<br>GPIO1_TSRL[8:9]=0b10 |

*Table 10. DMA Controller (DMA2P40) Interface*

| PPC460EX Signals | Ball | DMA2P40 | I/O | Configuration |
|---|---|---|---|---|
| [DMAReq3]GPIO33[PerPar3][IRQ4] | F13 | DMAReq3 | I | GPIO1_TSRL[2:3]=0b10<br>GPIO1_ISR2L[2:3]=0b01 |
| [EOT3/TC3]GPIO37[UART0RTS][UART3Tx] | D33 | EOT3/TC3 | I/O | GPIO1_OSRL[10:11]=0b10<br>GPIO1_TSRL[10:11]=0b10<br>GPIO1_ISR2L[10:11]=0b01<br><br>To enable EOT, set DMA2P40_CR3[ETD]=0. EOT is an input.<br><br>To enable TC, set DMA2P40_CR3[ETD]=1. TC is an output. |

**Note:** See errata before using DMA Interface.

*Table 11. EBC Interface*

| PPC460EX Signals | Ball | EBC0 | I/O | Configuration |
|---|---|---|---|---|
| [PerAddr05]GPIO46[DMAReq0][IRQ13] | B32 | PerAddr05 | O | GPIO1_OSRL[28:29]=0b01<br>GPIO1_TSRL[28:29]=0b01<br><br>A pull-up is required when connected to the boot rom. |
| [PerAddr06]GPIO47[DMAAck0][IRQ14] | C31 | PerAddr06 | O | GPIO1_OSRL[30:31]=0b01<br>GPIO1_TSRL[30:31]=0b01<br><br>A pull-up is required when connected to the boot rom. |
| [PerAddr07]GPIO48[EOT0/TC0][IRQ15] | D30 | PerAddr07 | O | GPIO1_OSRH[0:1]=0b01<br>GPIO1_TSRH[0:1]=0b01<br><br>A pull-up is required when connected to the boot rom. |

*Table 11. EBC Interface*

| PPC460EX Signals | Ball | EBC0 | I/O | Configuration |
|---|---|---|---|---|
| PerAddr08<br>PerAddr09<br>PerAddr10<br>PerAddr11<br>PerAddr12<br>PerAddr13<br>PerAddr14<br>PerAddr15<br>PerAddr16<br>PerAddr17<br>PerAddr18<br>PerAddr19<br>PerAddr20<br>PerAddr21<br>PerAddr22<br>PerAddr23<br>PerAddr24<br>PerAddr25<br>PerAddr26<br>PerAddr27<br>PerAddr28<br>PerAddr29<br>PerAddr30<br>PerAddr31 | A32<br>E29<br>C30<br>B31<br>A30<br>A31<br>D29<br>C29<br>A29<br>D28<br>C28<br>B29<br>C27<br>A28<br>D26<br>F27<br>B27<br>D27<br>A27<br>C26<br>A26<br>C25<br>B25<br>D24 | PerAddr08<br>PerAddr09<br>PerAddr10<br>PerAddr11<br>PerAddr12<br>PerAddr13<br>PerAddr14<br>PerAddr15<br>PerAddr16<br>PerAddr17<br>PerAddr18<br>PerAddr19<br>PerAddr20<br>PerAddr21<br>PerAddr22<br>PerAddr23<br>PerAddr24<br>PerAddr25<br>PerAddr26<br>PerAddr27<br>PerAddr28<br>PerAddr29<br>PerAddr30<br>PerAddr31 | O | PerAdd05 - MSb<br>PerAddr31 - LSb |
| $\overline{\text{PerBLast}}$ | F25 | $\overline{\text{PerBLast}}$ | O | |
| PerClk | F23 | PerClk | O | |
| $\overline{\text{PerCS0}}$[NFCE0] | E24 | $\overline{\text{PerCS0}}$ | O | SDR0_CUST0[NCG0]=0<br>Use $\overline{\text{PerCS0}}$ when booting from NOR flash. |
| [$\overline{\text{PerCS1}}$]GPIO41[$\overline{\text{NFCE1}}$] | B22 | $\overline{\text{PerCS1}}$ | O | SDR0_CUST0[NCG1]=0<br>GPIO1_OSRL[18:19]=0b01<br>GPIO1_TSRL[18:19]=0b01<br><br>Pull up required when used as a chip select. |
| [$\overline{\text{PerCS2}}$]GPIO42[$\overline{\text{NFCE2}}$] | D25 | $\overline{\text{PerCS2}}$ | O | SDR0_CUST0[NCG2]=0<br>GPIO1_OSRL[20:21]=0b01<br>GPIO1_TSRL[20:21]=0b01<br><br>Pull up required when used as a chip select. |
| [$\overline{\text{PerCS3}}$]GPIO43[$\overline{\text{NFCE3}}$][DMAReq1][IRQ10] | A22 | $\overline{\text{PerCS3}}$ | O | SDR0_CUST0[NCG3]=0<br>GPIO1_OSRL[22:23]=0b01<br>GPIO1_TSRL[22:23]=0b01<br><br>Pull up required when used as a chip select. |
| [$\overline{\text{PerCS4}}$]GPIO44[DMAAck1][IRQ11] | E21 | $\overline{\text{PerCS4}}$ | O | GPIO1_OSRL[24:25]=0b01<br>GPIO1_TSRL[24:25]=0b01<br><br>Pull up required when used as a chip select. |

*Table 11. EBC Interface*

| PPC460EX Signals | Ball | EBC0 | I/O | Configuration |
|---|---|---|---|---|
| [PerCS5]GPIO45[EOT1/TC1][IRQ12] | D21 | PerCS5 | O | GPIO1_OSRL[26:27]=0b01 GPIO1_TSRL[26:27]=0b01<br><br>Pull up required when used as a chip select. |
| PerData00 | C21 | PerData00 | | |
| PerData01 | B21 | PerData01 | | |
| PerData02 | A21 | PerData02 | | |
| PerData03 | E20 | PerData03 | | |
| PerData04 | D20 | PerData04 | | PerData00 - MSb |
| PerData05 | C20 | PerData05 | | PerData31 - LSb |
| PerData06 | D18 | PerData06 | | |
| PerData07 | B20 | PerData07 | | The EBC and NDFC share the PerData signals. |
| PerData08 | E19 | PerData08 | | The function on these signals depends on which |
| PerData09 | D19 | PerData09 | | controller controls the interface. |
| PerData10 | E18 | PerData10 | | |
| PerData11 | C19 | PerData11 | | • Connect PerData00:07 to 8 bit devices. |
| PerData12 | A19 | PerData12 | | PerData00 is the MSb and PerData07 is |
| PerData13 | C18 | PerData13 | | the LSb. PerData00 should be connected |
| PerData14 | B18 | PerData14 | | to boot rom data pin 7 and PerData 07 |
| PerData15 | A18 | PerData15 | I/O | should be connected to boot rom data pin |
| PerData16 | D17 | PerData16 | | 0. |
| PerData17 | B17 | PerData17 | | • Connect PerData00:15 to 16 bit devices. |
| PerData18 | A15 | PerData18 | | PerData00 is the MSb and PerData15 is |
| PerData19 | B15 | PerData19 | | the LSb. PerData00 should be connected |
| PerData20 | E15 | PerData20 | | to boot rom data pin 15 and PerData 15 |
| PerData21 | C15 | PerData21 | | should be connected to boot rom data pin |
| PerData22 | D16 | PerData22 | | 0. |
| PerData23 | D15 | PerData23 | | • Connect PerData00:31 to 32 bit devices. |
| PerData24 | E16 | PerData24 | | PerData00 is the MSb and PerData31 is |
| PerData25 | C14 | PerData25 | | the LSb. |
| PerData26 | E14 | PerData26 | | |
| PerData27 | D14 | PerData27 | | • 8-bit,16-bit and 32-bit boot devices are |
| PerData28 | B14 | PerData28 | | supported. |
| PerData29 | A13 | PerData29 | | |
| PerData30 | B13 | PerData30 | | |
| PerData31 | C13 | PerData31 | | |
| [PerPar0]GPIO30[DMAReq2][IRQ7] | A20 | PerPar0 | I/O | GPIO0_OSRH[28:29]=0b01 GPIO0_TSRH[28:29]=0b01 GPIO0_ISR1H[28:29]=0b01 |
| [PerPar1]GPIO31[DMAAck2][IRQ8] | A16 | PerPar1 | I/O | GPIO0_OSRH[30:31]=0b01 GPIO0_TSRH[30:31]=0b01 GPIO0_ISR1H[30:31]=0b01 |
| [PerPar2]GPIO32[EOT2/TC2][IRQ9] | A14 | PerPar2 | I/O | GPIO1_OSRL[0:1]=0b01 GPIO1_TSRL[0:1]=0b01 GPIO1_ISR1L[0:1]=0b01 |
| [PerPar3]GPIO33[DMAReq3][IRQ4] | F13 | PerPar3 | I/O | GPIO1_OSRL[2:3]=0b01 GPIO1_TSRL[2:3]=0b01 GPIO1_ISR1L[2:3]=0b01 |
| PerErr | D13 | PerErr | I | A pull down is required |
| PerOE | E26 | PerOE | O | |

*Table 11. EBC Interface*

| PPC460EX Signals | Ball | EBC0 | I/O | Configuration |
|---|---|---|---|---|
| PerReady | C17 | PerReady | I | EBC0_BnAP[RE]=1 (Reset default: EBC0_BnAP[RE]=0) |
| PerR/$\overline{W}$ | D23 | PerR/$\overline{W}$ | O | |
| $\overline{PerWBE0}$ $\overline{PerWBE1}$ $\overline{PerWBE2}$ $\overline{PerWBE3}$ | C23 A23 D22 C22 | $\overline{PerWBE0}$ $\overline{PerWBE1}$ $\overline{PerWBE2}$ $\overline{PerWBE3}$ | O | |
| $\overline{ExtReset}$ | F22 | $\overline{ExtReset}$ | O | If using $\overline{ExtReset}$ to reset the boot memory, ensure there is adequate setup time between ExReset and the first access. The first PerCS0 when booting occurs approximately 500ns after ExtReset deasserts (transitions from low to high). |

*Table 12. Ethernet - MII Signal Configuration*

| PPC460EX Signals | Ball | MII | I/O | Configuration |
|---|---|---|---|---|
| GMCMDClk | AJ03 | GMCMDClk | O | SDR0_ETH_CFG[MDIO_SEL]=00 |
| GMCMDIO | AK01 | GMCMDIO | I/O | The MDIO interface must be accessed through the EMAC0_STACR register. |
| GMCRefClk | AP09 | GMCRefClk | I | 125MHz reference clock only required when MII configured through the RGMII bridge. See Table 2. |
| GMC0CD, GMC1RxClk | AP05 | GMC0CD | I | |
| GMC0CrS, GMC1TxClk | AL07 | GMC0CrS | I | |
| GMC0RxClk, GMC0RxClk | AM07 | GMC0RxClk | I | |
| GMC0RxD0, GMC1RxD0 GMC0RxD1, GMC1RxD1 GMC0RxD2, GMC1RxD2 GMC0RxD3, GMC1RxD3 | AL09 AK09 AP08 AJ09 | GMC0RxD0 GMC0RxD1 GMC0RxD2 GMC0RxD3 | I | |
| GMC0RxDV, GMC0RxCtl | AL06 | GMC0RxDV | I | |
| GMC0RxEr, GMC1RxCtl | AJ10 | GMC0RxEr | I | |
| GMC0TxClk | AN04 | GMC0TxClk | I | |
| GMC0TxD0, GMC1TxD0 GMC0TxD1, GMC1TxD1 GMC0TxD2, GMC1TxD2 GMC0TxD3, GMC1TxD3 | AM02 AK04 AL02 AL01 | GMC0TxD0 GMC0TxD1 GMC0TxD2 GMC0TxD3 | O | |
| GMC0TxEn, GMC0TxCtl | AM05 | GMC0TxEn | O | |
| GMC0TxEr, GMC1TxCtl | AJ08 | GMC0TxEr | O | |

*Table 13. Ethernet - GMII Signal Configuration*

| PPC460EX Signals | Ball | GMII | I/O | Configuration |
|---|---|---|---|---|
| GMCMDClk | AJ03 | GMCMDClk | O | SDR0_ETH_CFG[MDIO_SEL]=00 |
| GMCMDIO | AK01 | GMCMDIO | I/O | The MDIO interface must be accessed through the EMAC0_STACR register. |
| GMCRefClk | AP09 | GMCRefClk | I | 125MHz reference clock |
| GMC0CD, GMC1RxClk | AP05 | GMC0CD | I | |
| GMC0CrS, GMC1TxClk | AL07 | GMC0CrS | I | |
| GMC0RxClk, GMC0RxClk | AM07 | GMC0RxClk | I | |
| GMC0RxD0, GMC1RxD0<br>GMC0RxD1, GMC1RxD1<br>GMC0RxD2, GMC1RxD2<br>GMC0RxD3, GMC1RxD3<br>GMC0RxD4, GMC1RxD0<br>GMC0RxD5, GMC1RxD1<br>GMC0RxD6, GMC1RxD2<br>GMC0RxD7, GMC1RxD3 | AL09<br>AK09<br>AP08<br>AJ09<br>AN08<br>AL08<br>AM08<br>AP07 | GMC0RxD0<br>GMC0RxD1<br>GMC0RxD2<br>GMC0RxD3<br>GMC0RxD4<br>GMC0RxD5<br>GMC0RxD6<br>GMC0RxD7 | I | |
| GMC0RxDV, GMC0RxCtl | AL06 | GMC0RxDV | I | |
| GMC0RxEr, GMC1RxCtl | AJ10 | GMC0RxEr | I | |
| GMC0GTxClk, GMC0TxClk | AN06 | GMC0GTxClk | O | |
| GMC0TxClk | AN04 | GMC0TxClk | I | |
| GMC0TxD0, GMC1TxD0<br>GMC0TxD1, GMC1TxD1<br>GMC0TxD2, GMC1TxD2<br>GMC0TxD3, GMC1TxD3<br>GMC0TxD4, GMC1TxD0<br>GMC0TxD5, GMC1TxD1<br>GMC0TxD6, GMC1TxD2<br>GMC0TxD7, GMC1TxD3 | AM02<br>AK04<br>AL02<br>AL01<br>AK03<br>AM01<br>AH05<br>AL03 | GMC0TxD0<br>GMC0TxD1<br>GMC0TxD2<br>GMC0TxD3<br>GMC0TxD4<br>GMC0TxD5<br>GMC0TxD6<br>GMC0TxD7 | O | |
| GMC0TxEn, GMC0TxCtl | AM05 | GMC0TxEn | O | |
| GMC0TxEr, GMC1TxCtl | AJ08 | GMC0TxEr | O | |

*Table 14. Ethernet - RGMII Signal Configuration*

| PPC460EX Signals | Ball | RGMII | I/O | Configuration |
|---|---|---|---|---|
| GMCMDClk | AJ03 | GMCMDClk | O | SDR0_ETH_CFG[MDIO_SEL]=00 |
| GMCMDIO | AK01 | GMCMDIO | I/O | The MDIO interface must be accessed through the EMAC0_STACR register. |
| GMCRefClk | AP09 | GMCRefClk | I | 125MHz reference clock for RGMII0 and RGMII1 |
| *RGMII0* | | | | |
| GMC0RxClk, GMC0RxClk | AM07 | GMC0RxClk | I | GMC0RxClk required by EMAC0 and EMAC1. Without GMC0RxClk, EMAC0 (RGMII0) and EMAC1 (RGMII1) cannot reset. On systems only using RGMII1, connect the RxClk from the RGMII1 PHY to GMC0RxClk and GMC1RxClk. On systems with RGMII0 and RGMII1 PHY, care must be taken that the RGMII0 PHY does not go into a low power state removing GMC0RxClk. |
| GMC0RxDV, GMC0RxCtl | AL06 | GMC0RxCtl | I | |
| GMC0RxD0, GMC0RxD0<br>GMC0RxD1, GMC0RxD1<br>GMC0RxD2, GMC0RxD2<br>GMC0RxD3, GMC0RxD3 | AL09<br>AK09<br>AP08<br>AJ09 | GMC0RxD0<br>GMC0RxD1<br>GMC0RxD2<br>GMC0RxD3 | I | |
| GMC0GTxClk, GMC0TxClk | AN06 | GMC0TxClk | O | |
| GMC0TxEn, GMC0TxCtl | AM05 | GMC0TxCtl | O | |
| GMC0TxD0, GMC0TxD0<br>GMC0TxD1, GMC0TxD1<br>GMC0TxD2, GMC0TxD2<br>GMC0TxD3, GMC0TxD3 | AM02<br>AK04<br>AL02<br>AL01 | GMC0TxD0<br>GMC0TxD1<br>GMC0TxD2<br>GMC0TxD3 | O | |
| *RGMII1* | | | | |
| GMC0CD, GMC1RxClk | AP05 | GMC1RxClk | I | GMC0RxClk is required to reset EMAC1. See configuration comments for RGMII0 GMC0RxClk. |
| GMC0RxEr, GMC1RxCtl | AJ10 | GMC1RxCtl | I | |
| GMC0RxD4, GMC1RxD0<br>GMC0RxD5, GMC1RxD1<br>GMC0RxD6, GMC1RxD2<br>GMC0RxD7, GMC1RxD3 | AN08<br>AL08<br>AM08<br>AP07 | GMC1RxD0<br>GMC1RxD1<br>GMC1RxD2<br>GMC1RxD3 | I | |
| GMC0CrS, GMC1TxClk | AL07 | GMC1TxClk | O | |
| GMC0TxEr, GMC1TxCtl | AJ08 | GMC1TxCtl | O | |
| GMC0TxD4, GMC1TxD0<br>GMC0TxD5, GMC1TxD1<br>GMC0TxD6, GMC1TxD2<br>GMC0TxD7, GMC1TxD3 | AK03<br>AM01<br>AH05<br>AL03 | GMC1TxD0<br>GMC1TxD1<br>GMC1TxD2<br>GMC1TxD3 | O | |

*Table 15. Ethernet - SGMII Signal Configuration*

| PPC460EX Signals | Ball | SGMII | I/O | Configuration |
|---|---|---|---|---|
| GMCMDClk | AJ03 | GMCMDClk | O | SDR0_ETH_CFG[MDIO_SEL]=00 |
| GMCMDIO | AK01 | GMCMDIO | I/O | The MDIO interface must be accessed through the EMAC0_STACR register.<br><br>When accessing the internal GPSC registers EMAC0_STACR must be used for EMAC0 and EMAC1_STACR for EMAC1. Access to the internal GPSC registers is not dependent on SDR0_ETH_CFG[MDIO_SEL]. |
| GMCRefClk | AP09 | GMCRefClk | I | GMCRefClk is a single ended 125MHz reference clock required reference clock for SGMII0 and SGMII1. |
| SGMIITxClk | AJ12 | SGMIITxClk | O | SGMII TxClk for SGMII0 and SGMII1. SGMII0TxClk/SGMII0TxClk is a 1.8V LVDS driver. A 100 ohm terminator required between the differential inputs of the far-end receiver. |
| $\overline{\text{SGMIITxClk}}$ | AK12 | $\overline{\text{SGMIITxClk}}$ | O | |
| *SGMII0* | | | | |
| SGMII0RxClk | AK15 | SGMII0RxClk | I | The receiver clock, SGMII0RxClk, must be connected. Clock recovery from the SGMII0RxD/SGMII0RxD signals is not supported. |
| $\overline{\text{SGMII0RxClk}}$ | AL15 | $\overline{\text{SGMII0RxClk}}$ | I | SGMII0RxClk/$\overline{\text{SGMII0RxClk}}$ is an unbiased 1.8V LVDS receiver with internal 100 Ohm termination. |
| SGMII0RxD | AN14 | SGMII0RxD | I | SGMII0RxD$\overline{\text{SGMII0RxD}}$ is an unbiased 1.8V LVDS receiver with 100 Ohm internal termination. |
| $\overline{\text{SGMII0RxD}}$ | AP14 | $\overline{\text{SGMII0RxD}}$ | I | |
| SGMII0TxD | AM11 | SGMII0TxD | O | SGMII0TxD/$\overline{\text{SGMII0TxD}}$ is a 1.8V LVDS driver. A 100 ohm terminator required between the differential inputs of the far-end receiver. |
| $\overline{\text{SGMII0TxD}}$ | AN11 | $\overline{\text{SGMII0TxD}}$ | O | |
| *SGMII1* | | | | |
| SGMII1RxClk | AL14 | SGMII1RxClk | I | The receiver clock, SGMII0RxClk, must be connected. Clock recovery from the SGMII1RxD/SGMII1RxD signals is not supported. |
| $\overline{\text{SGMII1RxClk}}$ | AM14 | $\overline{\text{SGMII1RxClk}}$ | I | SGMII1RxClk/$\overline{\text{SGMII1RxClk}}$ is an unbiased 1.8V LVDS receiver with internal 100 Ohm termination. |
| SGMII1RxD | AN13 | SGMII1RxD | I | SGMII1RxD/$\overline{\text{SGMII1RxD}}$ is an unbiased 1.8V LVDS receiver with 100 Ohm internal termination. |
| $\overline{\text{SGMII1RxD}}$ | AP13 | $\overline{\text{SGMII1RxD}}$ | I | |
| SGMII1TxD | AK11 | SGMII1TxD | O | SGMII0TxD/$\overline{\text{SGMII0TxD}}$ is a 1.8V LVDS driver. A 100 ohm terminator required between the differential inputs of the far-end receiver. |
| $\overline{\text{SGMII1TxD}}$ | AL11 | $\overline{\text{SGMII1TxD}}$ | O | |

**Note:** See errata before using SGMII.

*Table 16. GPIO00-31*

| PPC460EX Signals | Ball | GPIO | I/O | Configuration |
|---|---|---|---|---|
| GPIO00[USB2HD0] | AG01 | GPIO00 | I/O | GPIO0_OSRL[0:1]=0b00<br>GPIO0_TSRL[0:1]=0b00<br>GPIO0_ODR[0]=0<br>To drive 0:GPIO0_OR[0]=0,GPIO0_TCR[0]=1<br>To drive 1:GPIO0_OR[0]=1,GPIO0_TCR[0]=1<br>To place in HighZ: GPIO0_TCR[0]=0<br>To receive: Read GPIO0_IR[0] |
| GPIO01[USB2HD1] | AD05 | GPIO01 | I/O | GPIO0_OSRL[2:3]=0b00<br>GPIO0_TSRL[2:3]=0b00<br>GPIO0_ODR[1]=0<br>To drive 0:GPIO0_OR[1]=0,GPIO0_TCR[1]=1<br>To drive 1:GPIO0_OR[1]=1,GPIO0_TCR[1]=1<br>To place in HighZ: GPIO0_TCR[1]=0<br>To receive: Read GPIO0_IR[1] |
| GPIO02[USB2HD2] | AE04 | GPIO02 | I/O | GPIO0_OSRL[4:5]=0b00<br>GPIO0_TSRL[4:5]=0b00<br>GPIO0_ODR[2]=0<br>To drive 0:GPIO0_OR[2]=0, GPIO0_TCR[2]=1<br>To drive 1:GPIO0_OR[2]=1, GPIO0_TCR[2]=1<br>To place in HighZ: GPIO0_TCR[2]=0<br>To receive: Read GPIO0_IR[2] |
| GPIO03[USB2HD3] | AF01 | GPIO03 | I/O | GPIO0_OSRL[6:7]=0b00<br>GPIO0_TSRL[6:7]=0b00<br>GPIO0_ODR[3]=0<br>To drive 0:GPIO0_OR[3]=0,GPIO0_TCR[3]=1<br>To drive 1:GPIO0_OR[3]=1,GPIO0_TCR[3]=1<br>To place in HighZ: GPIO0_TCR[3]=0<br>To receive: Read GPIO0_IR[3] |
| GPIO04[USB2HD4] | AE02 | GPIO04 | I/O | GPIO0_OSRL[8:9]=0b00<br>GPIO0_TSRL[8:9]=0b00<br>GPIO0_ODR[4]=0<br>To drive 0:GPIO0_OR[4]=0,GPIO0_TCR[4]=1<br>To drive 1:GPIO0_OR[4]=1,GPIO0_TCR[4]=1<br>To place in HighZ: GPIO0_TCR[4]=0<br>To receive: Read GPIO0_IR[4] |
| GPIO05[USB2HD5] | AE01 | GPIO05 | I/O | GPIO0_OSRL[10:11]=0b00<br>GPIO0_TSRL[10:11]=0b00<br>GPIO0_ODR[5]=0<br>To drive 0:GPIO0_OR[5]=0,GPIO0_TCR[5]=1<br>To drive 1:GPIO0_OR[5]=1,GPIO0_TCR[5]=1<br>To place in HighZ: GPIO0_TCR[5]=0<br>To receive: Read GPIO0_IR[5] |
| GPIO06[USB2HD6] | AB05 | GPIO06 | I/O | GPIO0_OSRL[12:13]=0b00<br>GPIO0_TSRL[12:13]=0b00<br>GPIO0_ODR[6]=0<br>To drive 0:GPIO0_OR[6]=0,GPIO0_TCR[6]=1<br>To drive 1:GPIO0_OR[6]=1,GPIO0_TCR[6]=1<br>To place in HighZ: GPIO0_TCR[6]=0<br>To receive: Read GPIO0_IR[6] |

*Table 16. GPIO00-31*

| PPC460EX Signals | Ball | GPIO | I/O | Configuration |
|---|---|---|---|---|
| GPIO07[USB2HD7] | AD03 | GPIO07 | I/O | GPIO0_OSRL[14:15]=0b00<br>GPIO0_TSRL[14:15]=0b00<br>GPIO0_ODR[7]=0<br>To drive 0:GPIO0_OR[7]=0,GPIO0_TCR[7]=1<br>To drive 1:GPIO0_OR[7]=1,GPIO0_TCR[7]=1<br>To place in HighZ: GPIO0_TCR[7]=0<br>To receive: Read GPIO0_IR[7] |
| GPIO08[USB2DD0] | AH04 | GPIO08 | I/O | GPIO0_OSRL[16:17]=0b00<br>GPIO0_TSRL[16:17]=0b00<br>GPIO0_ODR[8]=0<br>To drive 0:GPIO0_OR[8]=0,GPIO0_TCR[8]=1<br>To drive 1:GPIO0_OR[8]=1,GPIO0_TCR[8]=1<br>To place in HighZ: GPIO0_TCR[8]=0<br>To receive: Read GPIO0_IR[8] |
| GPIO09[USB2DD1] | AJ05 | GPIO09 | I/O | GPIO0_OSRL[18:19]=0b00<br>GPIO0_TSRL[18:19]=0b00<br>GPIO0_ODR[9]=0<br>To drive 0:GPIO0_OR[9]=0,GPIO0_TCR[9]=1<br>To drive 1:GPIO0_OR[9]=1,GPIO0_TCR[9]=1<br>To place in HighZ: GPIO0_TCR[9]=0<br>To receive: Read GPIO0_IR[9] |
| GPIO10[USB2DD2] | AG06 | GPIO10 | I/O | GPIO0_OSRL[20:21]=0b00<br>GPIO0_TSRL[20:21]=0b00<br>GPIO0_ODR[10]=0<br>To drive 0:GPIO0_OR[10]=0,GPIO0_TCR[10]=1<br>To drive 1:GPIO0_OR[10]=1,GPIO0_TCR[10]=1<br>To place in HighZ: GPIO0_TCR[10]=0<br>To receive: Read GPIO0_IR[10] |
| GPIO11[USB2DD3] | AJ02 | GPIO11 | I/O | GPIO0_OSRL[22:23]=0b00<br>GPIO0_TSRL[22:23]=0b00<br>GPIO0_ODR[11]=0<br>To drive 0:GPIO0_OR[11]=0,GPIO0_TCR[11]=1<br>To drive 1:GPIO0_OR[11]=1,GPIO0_TCR[11]=1<br>To place in HighZ: GPIO0_TCR[11]=0<br>To receive: Read GPIO0_IR[11] |
| GPIO12[USB2DD4] | AJ04 | GPIO12 | I/O | GPIO0_OSRL[24:25]=0b00<br>GPIO0_TSRL[24:25]=0b00<br>GPIO0_ODR[12]=0<br>To drive 0:GPIO0_OR[12]=0,GPIO0_TCR[12]=1<br>To drive 1:GPIO0_OR[12]=1,GPIO0_TCR[12]=1<br>To place in HighZ: GPIO0_TCR[12]=0<br>To receive: Read GPIO0_IR[12] |
| GPIO13[USB2DD5] | AH03 | GPIO13 | I/O | GPIO0_OSRL[26:27]=0b00<br>GPIO0_TSRL[26:27]=0b00<br>GPIO0_ODR[13]=0<br>To drive 0:GPIO0_OR[13]=0,GPIO0_TCR[13]=1<br>To drive 1:GPIO0_OR[13]=1,GPIO0_TCR[13]=1<br>To place in HighZ: GPIO0_TCR[13]=0<br>To receive: Read GPIO0_IR[13] |

*Table 16. GPIO00-31*

| PPC460EX Signals | Ball | GPIO | I/O | Configuration |
|---|---|---|---|---|
| GPIO14[USB2DD6] | AJ01 | GPIO14 | I/O | GPIO0_OSRL[28:29]=0b00<br>GPIO0_TSRL[28:29]=0b00<br>GPIO0_ODR[14]=0<br>To drive 0:GPIO0_OR[14]=0,GPIO0_TCR[14]=1<br>To drive 1:GPIO0_OR[14]=1,GPIO0_TCR[14]=1<br>To place in HighZ: GPIO0_TCR[14]=0<br>To receive: Read GPIO0_IR[14] |
| GPIO15[USB2DD7] | AH01 | GPIO15 | I/O | GPIO0_OSRL[30:31]=0b00<br>GPIO0_TSRL[30:31]=0b00<br>GPIO0_ODR[15]=0<br>To drive 0:GPIO0_OR[15]=0,GPIO0_TCR[15]=1<br>To drive 1:GPIO0_OR[15]=1,GPIO0_TCR[15]=1<br>To place in HighZ: GPIO0_TCR[15]=0<br>To receive: Read GPIO0_IR[15] |
| GPIO16[USB2HStop] | AF04 | GPIO16 | I/O | GPIO0_OSRH[0:1]=0b00<br>GPIO0_TSRH[0:1]=0b00<br>GPIO0_ODR[16]=0]<br>To drive 0:GPIO0_OR[16]=0,GPIO0_TCR[16=1<br>To drive 1:GPIO0_OR[16]=1,GPIO0_TCR[16]=1<br>To place in HighZ: GPIO0_TCR[16]=0<br>To receive: Read GPIO0_IR[16] |
| GPIO17[USB2HNext] | AG02 | GPIO17 | I/O | GPIO0_OSRH[2:3]=0b00<br>GPIO0_TSRH[2:3]=0b00<br>GPIO0_ODR[17]=0<br>To drive 0:GPIO0_OR[17]=0,GPIO0_TCR[17]=1<br>To drive 1:GPIO0_OR[17]=1,GPIO0_TCR[17]=1<br>To place in HighZ: GPIO0_TCR[17]=0<br>To receive: Read GPIO0_IR[17] |
| GPIO18[USB2HDir] | AG04 | GPIO18 | I/O | GPIO0_OSRH[4:5]=0b00<br>GPIO0_TSRH[4:5]=0b00<br>GPIO0_ODR[18]=0<br>To drive 0:GPIO0_OR[18]=0,GPIO0_TCR[18]=1<br>To drive 1:GPIO0_OR[18]=1,GPIO0_TCR[18]=1<br>To place in HighZ: GPIO0_TCR[18]=0<br>To receive: Read GPIO0_IR[18] |
| GPIO19[USB2DStop] | AF03 | GPIO19 | I/O | GPIO0_OSRH[6:7]=0b00<br>GPIO0_TSRH[6:7]=0b00<br>GPIO0_ODR[19]=0<br>To drive 0:GPIO0_OR[19]=0,GPIO0_TCR[19]=1<br>To drive 1:GPIO0_OR[19]=1,GPIO0_TCR[19]=1<br>To place in HighZ: GPIO0_TCR[19]=0<br>To receive: Read GPIO0_IR[19] |
| GPIO20[USB2DNext] | AG03 | GPIO20 | I/O | GPIO0_OSRH[8:9]=0b00<br>GPIO0_TSRH[8:9]=0b00<br>GPIO0_ODR[20]=0<br>To drive 0:GPIO0_OR[20]=0,GPIO0_TCR[20]=1<br>To drive 1:GPIO0_OR[20]=1,GPIO0_TCR[20]=1<br>To place in HighZ: GPIO0_TCR[20]=0<br>To receive: Read GPIO0_IR[20] |

*Table 16. GPIO00-31*

| PPC460EX Signals | Ball | GPIO | I/O | Configuration |
|---|---|---|---|---|
| GPIO21[USB2DDir] | AD04 | GPIO21 | I/O | GPIO0_OSRH[10:11]=0b00<br>GPIO0_TSRH[10:11]=0b00<br>GPIO0_ODR[21]=0<br>To drive 0:GPIO0_OR[21]=0,GPIO0_TCR[21]=1<br>To drive 1:GPIO0_OR[21]=1,GPIO0_TCR[21]=1<br>To place in HighZ: GPIO0_TCR[21]=0<br>To receive: Read GPIO0_IR[21] |
| GPIO22[NFRdyBusy] | C24 | GPIO22 | I/O | GPIO0_OSRH[12:13]=0b00<br>GPIO0_TSRH[12:13]=0b00<br>GPIO0_ODR[22]=0<br>To drive 0:GPIO0_OR[22]=0,GPIO0_TCR[22]=1<br>To drive 1:GPIO0_OR[22]=1,GPIO0_TCR[22]=1<br>To place in HighZ: GPIO0_TCR[22]=0<br>To receive: Read GPIO0_IR[22] |
| GPIO23[NFREn] | B24 | GPIO23 | I/O | GPIO0_OSRH[14:15]=0b00<br>GPIO0_TSRH[14:15]=0b00<br>GPIO0_ODR[23]=0<br>To drive 0:GPIO0_OR[23]=0,GPIO0_TCR[23]=1<br>To drive 1:GPIO0_OR[23]=1,GPIO0_TCR[23]=1<br>To place in HighZ: GPIO0_TCR[23]=0<br>To receive: Read GPIO0_IR[23] |
| GPIO24[NFWEn] | A24 | GPIO24 | I/O | GPIO0_OSRH[16:17]=0b00<br>GPIO0_TSRH[16:17]=0b00<br>GPIO0_ODR[24]=0<br>To drive 0:GPIO0_OR[24]=0,GPIO0_TCR[24]=1<br>To drive 1:GPIO0_OR[24]=1,GPIO0_TCR[24]=1<br>To place in HighZ: GPIO0_TCR[24]=0<br>To receive: Read GPIO0_IR[24] |
| GPIO25[NFCLE] | F26 | GPIO25 | I/O | GPIO0_OSRH[18:19]=0b00<br>GPIO0_TSRH[18:19]=0b00<br>GPIO0_ODR[25]=0<br>To drive 0:GPIO0_OR[25]=0,GPIO0_TCR[25]=1<br>To drive 1:GPIO0_OR[25]=1,GPIO0_TCR[25]=1<br>To place in HighZ: GPIO0_TCR[25]=0<br>To receive: Read GPIO0_IR[25] |
| GPIO26[NFALE] | A25 | GPIO26 | I/O | GPIO0_OSRH[20:21]=0b00<br>GPIO0_TSRH[20:21]=0b00<br>GPIO0_ODR[26]=0<br>To drive 0:GPIO0_OR[26]=0,GPIO0_TCR[26]=1<br>To drive 1:GPIO0_OR[26]=1,GPIO0_TCR[26]=1<br>To place in HighZ: GPIO0_TCR[26]=0<br>To receive: Read GPIO0_IR[26] |
| GPIO27[IRQ0] | D12 | GPIO27 | I/O | GPIO0_OSRH[22:23]=0b00<br>GPIO0_TSRH[22:23]=0b00<br>GPIO0_ODR[2]7=0<br>To drive 0:GPIO0_OR[27]=0,GPIO0_TCR[27]=1<br>To drive 1:GPIO0_OR[27]=1,GPIO0_TCR[27]=1<br>To place in HighZ: GPIO0_TCR[27]=0<br>To receive: Read GPIO0_IR[27] |

*Table 16. GPIO00-31*

| PPC460EX Signals | Ball | GPIO | I/O | Configuration |
|---|---|---|---|---|
| GPIO28[IRQ1] | E12 | GPIO28 | I/O | GPIO0_OSRH[24:25]=0b00<br>GPIO0_TSRH[24:25]=0b00<br>GPIO0_ODR[28]=0<br>To drive 0:GPIO0_OR[28]=0,GPIO0_TCR[28]=1<br>To drive 1:GPIO0_OR[28]=1,GPIO0_TCR[28]=1<br>To place in HighZ: GPIO0_TCR[28]=0<br>To receive: Read GPIO0_IR[28] |
| GPIO29[IRQ2] | F12 | GPIO29 | I/O | GPIO0_OSRH[26:27]=0b00<br>GPIO0_TSRH[26:27]=0b00<br>GPIO0_ODR[29]=0<br>To drive 0:GPIO0_OR[29]=0,GPIO0_TCR[29]=1<br>To drive 1:GPIO0_OR[29]=1,GPIO0_TCR[29]=1<br>To place in HighZ: GPIO0_TCR[29]=0<br>To receive: Read GPIO0_IR[29] |
| GPIO30[PerPar0][DMAReq2][IRQ7] | A20 | GPIO30 | I/O | GPIO0_OSRH[28:29]=0b00<br>GPIO0_TSRH[28:29]=0b00<br>GPIO0_ODR[30]=0<br>To drive 0:GPIO0_OR[30]=0,GPIO0_TCR[30]=1<br>To drive 1:GPIO0_OR[30]=1,GPIO0_TCR[30]=1<br>To place in HighZ: GPIO0_TCR[30]=0<br>To receive: Read GPIO0_IR[30] |
| GPIO31[PerPar1][DMAAck2][IRQ8] | A16 | GPIO31 | I/O | GPIO0_OSRH[30:31]=0b00<br>GPIO0_TSRH[30:31]=0b00<br>GPIO0_ODR[31]=0<br>To drive 0:GPIO0_OR[31]=0,GPIO0_TCR[31]=1<br>To drive 1:GPIO0_OR[31]=1,GPIO0_TCR[31]=1<br>To place in HighZ: GPIO0_TCR[31]=0<br>To receive: Read GPIO0_IR[31] |

*Table 17. GPIO32-63*

| PPC460EX Signals | Ball | GPIO | I/O | Configuration |
|---|---|---|---|---|
| GPIO32[PerPar2][EOT2/TC2][IRQ9] | A14 | GPIO32 | I/O | GPIO1_OSRL[0:1]=0b00<br>GPIO1_TSRL[0:1]=0b00<br>GPIO1_ODR[0]=0<br>To drive 0:GPIO1_OR[0]=0,GPIO1_TCR[0]=1<br>To drive 1:GPIO1_OR[0]=1,GPIO1_TCR[0]=1<br>To place in HighZ: GPIO1_TCR[0]=0<br>To receive: Read GPIO0_IR[0] |
| GPIO33[PerPar3][DMAReq3][IRQ4] | F13 | GPIO33 | I/O | GPIO1_OSRL[2:3]=0b00<br>GPIO1_TSRL[2:3]=0b00<br>GPIO1_ODR[1]=0<br>To drive 0:GPIO1_OR[1]=0,GPIO1_TCR[1]=1<br>To drive 1:GPIO1_OR[1]=1,GPIO1_TCR[1]=1<br>To place in HighZ: GPIO1_TCR[1]=0<br>To receive: Read GPIO0_IR[1] |

*Table 17. GPIO32-63*

| PPC460EX Signals | Ball | GPIO | I/O | Configuration |
|---|---|---|---|---|
| GPIO34[UART0DCD][UART1CTS][UART2Tx] | E34 | GPIO34 | I/O | GPIO1_OSRL[4:5]=0b00<br>GPIO1_TSRL[4:5]=0b00<br>GPIO1_ODR[2]=0<br>To drive 0:GPIO1_OR[2]=0,GPIO1_TCR[2]=1<br>To drive 1:GPIO1_OR[2]=1,GPIO1_TCR[2]=1<br>To place in HighZ: GPIO1_TCR[2]=0<br>To receive: Read GPIO1_IR[2] |
| GPIO35[UART0DSR][UART1RTS][UART2Rx] | E32 | GPIO35 | I/O | GPIO1_OSRL[6:7]=0b00<br>GPIO1_TSRL[6:7]=0b00<br>GPIO1_ODR[3]=0<br>To drive 0:GPIO1_OR[3]=0,GPIO1_TCR[3]=1<br>To drive 1:GPIO1_OR[3]=1,GPIO1_TCR[3]=1<br>To place in HighZ: GPIO1_TCR[3]=0<br>To receive: Read GPIO1_IR[3] |
| GPIO36[UART0CTS][DMAAck3][UART3Rx] | E31 | GPIO36 | I/O | GPIO1_OSRL[8:9]=0b00<br>GPIO1_TSRL[8:9]=0b00<br>GPIO1_ODR[4]=0<br>To drive 0:GPIO1_OR[4]=0,GPIO1_TCR[4]=1<br>To drive 1:GPIO1_OR[4]=1,GPIO1_TCR[4]=1<br>To place in HighZ: GPIO1_TCR[4]=0<br>To receive: Read GPIO1_IR[4] |
| GPIO37[UART0RTS][EOT3/TC3][UART3Tx] | D33 | GPIO37 | I/O | GPIO1_OSRL[10:11]=0b00<br>GPIO1_TSRL[10:11]=0b00<br>GPIO1_ODR[5]=0<br>To drive 0:GPIO1_OR[5]=0,GPIO1_TCR[5]=1<br>To drive 1:GPIO1_OR[5]=1,GPIO1_TCR[5]=1<br>To place in HighZ: GPIO1_TCR[5]=0<br>To receive: Read GPIO1_IR[5] |
| GPIO38[UART0DTR][UART1Tx][IRQ5] | D32 | GPIO38 | I/O | GPIO1_OSRL[12:13]=0b00<br>GPIO1_TSRL[12:13]=0b00<br>GPIO1_ODR[6]=0<br>To drive 0:GPIO1_OR[6]=0,GPIO1_TCR[6]=1<br>To drive 1:GPIO1_OR[6]=1,GPIO1_TCR[6]=1<br>To place in HighZ: GPIO1_TCR[6]=0<br>To receive: Read GPIO1_IR[6] |
| GPIO39[UART0RI][UART1Rx][IRQ6] | D34 | GPIO39 | I/O | GPIO1_OSRL[14:15]=0b00<br>GPIO1_TSRL[14:15]=0b00<br>GPIO1_ODR[7]=0<br>To drive 0:GPIO1_OR[7]=0,GPIO1_TCR[7]=1<br>To drive 1:GPIO1_OR[7]=1,GPIO1_TCR[7]=1<br>To place in HighZ: GPIO1_TCR[7]=0<br>To receive: Read GPIO1_IR[7] |
| GPIO40[IRQ3] | C12 | GPIO40 | I/O | GPIO1_OSRL[16:17]=0b00<br>GPIO1_TSRL[16:17]=0b00<br>GPIO1_ODR[8]=0<br>To drive 0:GPIO1_OR[8]=0,GPIO1_TCR[8]=1<br>To drive 1:GPIO1_OR[8]=1,GPIO1_TCR[8]=1<br>To place in HighZ: GPIO1_TCR[8]=0<br>To receive: Read GPIO1_IR[8] |

*Application Note*

*Table 17. GPIO32-63*

| PPC460EX Signals | Ball | GPIO | I/O | Configuration |
|---|---|---|---|---|
| GPIO41[PerCS1][NFCE1] | B22 | GPIO41 | I/O | GPIO1_OSRL[18:19]=0b00<br>GPIO1_TSRL[18:19]=0b00<br>GPIO1_ODR[9]=0<br>To drive 0:GPIO1_OR[9]=0,GPIO1_TCR[9]=1<br>To drive 1:GPIO1_OR[9]=1,GPIO1_TCR[9]=1<br>To place in HighZ: GPIO1_TCR[9]=0<br>To receive: Read GPIO1_IR[9] |
| GPIO42[PerCS2][NFCE2] | D25 | GPIO42 | I/O | GPIO1_OSRL[20:21]=0b00<br>GPIO1_TSRL[20:21]=0b00<br>GPIO1_ODR[10]=0<br>To drive 0:GPIO1_OR[10]=0,GPIO1_TCR[10]=1<br>To drive 1:GPIO1_OR[10]=1,GPIO1_TCR[10]=1<br>To place in HighZ: GPIO1_TCR[10]=0<br>To receive: Read GPIO1_IR[10] |
| GPIO43[PerCS3][NFCE3][DMAReq1][IRQ10] | A22 | GPIO43 | I/O | GPIO1_OSRL[22:23]=0b00<br>GPIO1_TSRL[22:23]=0b00<br>GPIO1_ODR[11]=0<br>To drive 0:GPIO1_OR[11]=0,GPIO1_TCR[11]=1<br>To drive 1:GPIO1_OR[11]=1,GPIO1_TCR[11]=1<br>To place in HighZ: GPIO1_TCR[11]=0<br>To receive: Read GPIO1_IR[11] |
| GPIO44[PerCS4][DMAAck1][IRQ11] | E21 | GPIO44 | I/O | GPIO1_OSRL[24:25]=0b00<br>GPIO1_TSRL[24:25]=0b00<br>GPIO1_ODR[12]=0<br>To drive 0:GPIO1_OR[12]=0,GPIO1_TCR[12]=1<br>To drive 1:GPIO1_OR[12]=1,GPIO1_TCR[12]=1<br>To place in HighZ: GPIO1_TCR[12]=0<br>To receive: Read GPIO0_IR[12] |
| GPIO45[PerCS5][EOT1/TC1][IRQ12] | D21 | GPIO45 | I/O | GPIO1_OSRL[26:27]=0b00<br>GPIO1_TSRL[26:27]=0b00<br>GPIO1_ODR[13]=0<br>To drive 0:GPIO1_OR[13]=0,GPIO1_TCR[13]=1<br>To drive 1:GPIO1_OR[13]=1,GPIO1_TCR[13]=1<br>To place in HighZ: GPIO1_TCR[13]=0<br>To receive: Read GPIO1_IR[13] |
| GPIO46[PerAddr05][DMAReq0][IRQ13] | B32 | GPIO46 | I/O | GPIO1_OSRL[28:29]=0b00<br>GPIO1_TSRL[28:29]=0b00<br>GPIO1_ODR[14]=0<br>To drive 0:GPIO1_OR[14]=0,GPIO1_TCR[14=]1<br>To drive 1:GPIO1_OR[14]=1,GPIO1_TCR[14]=1<br>To place in HighZ: GPIO1_TCR[14]=0<br>To receive: Read GPIO1_IR[14] |
| GPIO47[PerAddr06][DMAAck0][IRQ14] | C31 | GPIO47 | I/O | GPIO1_OSRL[30:31]=0b00<br>GPIO1_TSRL[30:31]=0b00<br>GPIO1_ODR[15]=0<br>To drive 0:GPIO1_OR[15]=0,GPIO1_TCR[15]=1<br>To drive 1:GPIO1_OR[15]=1,GPIO1_TCR[15]=1<br>To place in HighZ: GPIO1_TCR[15]=0<br>To receive: Read GPIO1_IR[15] |

*Table 17. GPIO32-63*

| PPC460EX Signals | Ball | GPIO | I/O | Configuration |
|---|---|---|---|---|
| GPIO48[PerAddr07][EOT0/TC0][IRQ15] | D30 | GPIO48 | I/O | GPIO1_OSRH[0:1]=0b00<br>GPIO1_TSRH[0:1]=0b00<br>GPIO1_ODR[16]=0<br>To drive 0:GPIO1_OR[16]=0,GPIO1_TCR[16]=1<br>To drive 1:GPIO1_OR[16]=1,GPIO1_TCR[16]=1<br>To place in HighZ: GPIO1_TCR[16]=0<br>To receive: Read GPIO1_IR[16] |
| GPIO49[TrcBS0] | H33 | GPIO49 | I/O | SDR0_PFC0[DBG]=0<br>SDR0_PFC0[17:31]=0x7FFF<br>GPIO1_OSRH[2:3]=0b00<br>GPIO1_TSRH[2:3]=0b00<br>GPIO1_ODR[17]=0<br>To drive 0:GPIO1_OR[17]=0,GPIO1_TCR[17]=1<br>To drive 1:GPIO1_OR[17]=1,GPIO1_TCR[17]=1<br>To place in HighZ: GPIO1_TCR[17]=0<br>To receive: Read GPIO1_IR1[7] |
| GPIO50[TrcBS1] | J34 | GPIO50 | I/O | SDR0_PFC0[DBG]=0<br>SDR0_PFC0[17:31]=0x7FFF<br>GPIO1_OSRH[4:5]=0b00<br>GPIO1_TSRH[4:5]=0b00<br>GPIO1_ODR[18]=0<br>To drive 0:GPIO1_OR[18]=0,GPIO1_TCR[18]=1<br>To drive 1:GPIO1_OR[18]=1,GPIO1_TCR[18]=1<br>To place in HighZ: GPIO1_TCR[18]=0<br>To receive: Read GPIO1_IR[18] |
| GPIO51[TrcBS2] | H34 | GPIO51 | I/O | SDR0_PFC0[DBG]=0<br>SDR0_PFC0[17:31]=0x7FFF<br>GPIO1_OSRH[6:7]=0b00<br>GPIO1_TSRH[6:7]=0b00<br>GPIO1_ODR[19]=0<br>To drive 0:GPIO1_OR[19]=0,GPIO1_TCR[19]=1<br>To drive 1:GPIO1_OR[19]=1,GPIO1_TCR[19]=1<br>To place in HighZ: GPIO1_TCR[19]=0<br>To receive: Read GPIO1_IR[19] |
| GPIO52[TrcES0] | L30 | GPIO52 | I/O | SDR0_PFC0[DBG]=0<br>SDR0_PFC0[17:31]=0x7FFF<br>GPIO1_OSRH[8:9]=0b00<br>GPIO1_TSRH[8:9]=0b00<br>GPIO1_ODR[20]=0<br>To drive 0:GPIO1_OR[20]=0,GPIO1_TCR[20]=1<br>To drive 1:GPIO1_OR[20]=1,GPIO1_TCR[20]=1<br>To place in HighZ: GPIO1_TCR[20]=0<br>To receive: Read GPIO1_IR[20] |
| GPIO53[TrcES1] | L31 | GPIO53 | I/O | SDR0_PFC0[DBG]=0<br>SDR0_PFC0[17:31]=0x7FFF<br>GPIO1_OSRH[10:11]=0b00<br>GPIO1_TSRH[10:11]=0b00<br>GPIO1_ODR[21]=0<br>To drive 0:GPIO1_OR[21]=0,GPIO1_TCR[21]=1<br>To drive 1:GPIO1_OR[21]=1,GPIO1_TCR[21]=1<br>To place in HighZ: GPIO1_TCR[21]=0<br>To receive: Read GPIO1_IR[21] |

*Application Note*

*Table 17. GPIO32-63*

| PPC460EX Signals | Ball | GPIO | I/O | Configuration |
|---|---|---|---|---|
| GPIO54[TrcES2] | K33 | GPIO54 | I/O | SDR0_PFC0[DBG]=0<br>SDR0_PFC0[17:31]=0x7FFF<br>GPIO1_OSRH[12:13]=0b00<br>GPIO1_TSRH[12:13]=0b00<br>GPIO1_ODR[22]=0<br>To drive 0:GPIO1_OR[22]=0,GPIO1_TCR[22]=1<br>To drive 1:GPIO1_OR[22]=1,GPIO1_TCR[22]=1<br>To place in HighZ: GPIO1_TCR[22]=0<br>To receive: Read GPIO1_IR[22] |
| GPIO55[TrcES3] | L32 | GPIO55 | I/O | SDR0_PFC0[DBG]=0<br>SDR0_PFC0[17:31]=0x7FFF<br>GPIO1_OSRH[14:15]=0b00<br>GPIO1_TSRH[14:15]=0b00<br>GPIO1_ODR[23]=0<br>To drive 0:GPIO1_OR[23]=0,GPIO1_TCR[23]=1<br>To drive 1:GPIO1_OR[23]=1,GPIO1_TCR[23]=1<br>To place in HighZ: GPIO1_TCR[23]=0<br>To receive: Read GPIO1_IR[23] |
| GPIO56[TrcES4] | K34 | GPIO56 | I/O | SDR0_PFC0[DBG]=0<br>SDR0_PFC0[17:31]=0x7FFF<br>GPIO1_OSRH[16:17]=0b00<br>GPIO1_TSRH[16:17]=0b00<br>GPIO1_ODR[24]=0<br>To drive 0:GPIO1_OR[24]=0,GPIO1_TCR[24]=1<br>To drive 1:GPIO1_OR[24]=1,GPIO1_TCR[24]=1<br>To place in HighZ: GPIO1_TCR[24]=0<br>To receive: Read GPIO1_IR[24] |
| GPIO57[TrcTS0] | L33 | GPIO57 | I/O | SDR0_PFC0[DBG]=0<br>SDR0_PFC0[17:31]=0x7FFF<br>GPIO1_OSRH[18:19]=0b00<br>GPIO1_TSRH[18:19]=0b00<br>GPIO1_ODR[25]=0<br>To drive 0:GPIO1_OR[25]=0,GPIO1_TCR[25]=1<br>To drive 1:GPIO1_OR[25]=1,GPIO1_TCR[25]=1<br>To place in HighZ: GPIO1_TCR[25]=0<br>To receive: Read GPIO1_IR[25] |
| GPIO58[TrcTS1] | N29 | GPIO58 | I/O | SDR0_PFC0[DBG]=0<br>SDR0_PFC0[17:31]=0x7FFF<br>GPIO1_OSRH[20:21]=0b00<br>GPIO1_TSRH[20:21]=0b00<br>GPIO1_ODR[26]=0<br>To drive 0:GPIO1_OR[26]=0,GPIO1_TCR[26]=1<br>To drive 1:GPIO1_OR[26]=1,GPIO1_TCR[26]=1<br>To place in HighZ: GPIO1_TCR[26]=0<br>To receive: Read GPIO1_IR[26] |

*Application Note*

*Table 17. GPIO32-63*

| PPC460EX Signals | Ball | GPIO | I/O | Configuration |
|---|---|---|---|---|
| GPIO59[TrcTS2] | M31 | GPIO59 | I/O | SDR0_PFC0[DBG]=0<br>SDR0_PFC0[17:31]=0x7FFF<br>GPIO1_OSRH[22:23]=0b00<br>GPIO1_TSRH[22:23]=0b00<br>GPIO1_ODR[27]=0<br>To drive 0:GPIO1_OR[27]=0,GPIO1_TCR[27]=1<br>To drive 1:GPIO1_OR[27]=1,GPIO1_TCR[27]=1<br>To place in HighZ: GPIO1_TCR[27]=0<br>To receive: Read GPIO1_IR[27] |
| GPIO60[TrcTS3] | L34 | GPIO60 | I/O | SDR0_PFC0[DBG]=0<br>SDR0_PFC0[17:31]=0x7FFF<br>GPIO1_OSRH[24:25]=0b00<br>GPIO1_TSRH[24:25]=0b00<br>GPIO1_ODR[28]=0<br>To drive 0:GPIO1_OR[28]=0,GPIO1_TCR[28]=1<br>To drive 1:GPIO1_OR[28]=1,GPIO1_TCR[28]=1<br>To place in HighZ: GPIO1_TCR[28]=0<br>To receive: Read GPIO1_IR[28] |
| GPIO61[TrcTS4] | M32 | GPIO61 | I/O | SDR0_PFC0[DBG]=0<br>SDR0_PFC0[17:31]=0x7FFF<br>GPIO1_OSRH[26:27]=0b00<br>GPIO1_TSRH[26:27]=0b00<br>GPIO1_ODR[29]=0<br>To drive 0:GPIO1_OR[29]=0,GPIO1_TCR[29]=1<br>To drive 1:GPIO1_OR[29]=1,GPIO1_TCR[29]=1<br>To place in HighZ: GPIO1_TCR[29]=0<br>To receive: Read GPIO1_IR[29] |
| GPIO62[TrcTS5] | M34 | GPIO62 | I/O | SDR0_PFC0[DBG]=0<br>SDR0_PFC0[17:31]=0x7FFF<br>GPIO1_OSRH[28:29]=0b00<br>GPIO1_TSRH[28:29]=0b00<br>GPIO1_ODR[30]=0<br>To drive 0:GPIO1_OR[30]=0,GPIO1_TCR[30]=1<br>To drive 1:GPIO1_OR[30]=1,GPIO1_TCR[30]=1<br>To place in HighZ: GPIO1_TCR[30]=0<br>To receive: Read GPIO1_IR[30] |
| GPIO63[TrcTS6] | N31 | GPIO63 | I/O | SDR0_PFC0[DBG]=0<br>SDR0_PFC0[17:31]=0x7FFF<br>GPIO1_OSRH[30:31]=0b00<br>GPIO1_TSRH[30:31]=0b00<br>GPIO1_ODR[31]=0<br>To drive 0:GPIO1_OR[31]=0,GPIO1_TCR[31]=1<br>To drive 1:GPIO1_OR[31]=1,GPIO1_TCR[31]=1<br>To place in HighZ: GPIO1_TCR[31]=0<br>To receive: Read GPIO1_IR[31] |

*Table 18. IIC Interfaces*

| PPC460EX Signals | Ball | IIC | I/O | Configuration |
|---|---|---|---|---|
| *IIC0* | | | | |
| IIC0SCLK | J31 | IIC0SCLK | I/O | For Boot Option G or H, attach an I2C serial rom to IIC0. The I2C serial rom contains boot configurations such as clock settings and rom width. Select an I2C serial rom with a byte offset address (256 byte addressable I2C serial rom). Serial rom with multibyte offset addresses are not supported by Boot Option G or H.<br><br>Boot Option G - I2C address 0b1010100<br>Boot Option H - I2C address 0b1010010 |
| IIC0SData | H31 | IIC0SData | I/O | |
| *IIC1* | | | | |
| [IIC1SClk]SCPClkOut | K31 | IIC1SClk | I/0 | Set SDR0_PFC1[SIS]=1. |
| [IIC1SData]SCPDO | G34 | IIC1SData | I/0 | |

*Table 19. IRQ Signals*

| PPC460EX Signals | Ball | IRQ | I/O | Configuration |
|---|---|---|---|---|
| [IRQ0]GPIO27 | D12 | IRQ0 | I | GPIO0_TSRH[22:23]=0b01<br>GPIO0_ISR1H[22:23]=0b01 |
| [IRQ1]GPIO28 | E12 | IRQ1 | I | GPIO0_TSRH[24:25]=0b01<br>GPIO0_ISR1H[24:25]=0b01 |
| [IRQ2]GPIO29 | F12 | IRQ2 | I | GPIO0_TSRH[26:27]=0b01<br>GPIO0_ISR1H[26:27]=0b01 |
| [IRQ3]GPIO40 | C12 | IRQ3 | I | GPIO1_TSRL[16:17]=0b01<br>GPIO1_ISR1L[16:17]=0b01 |
| [IRQ4]GPIO33[PerPar3][DMAReq3] | F13 | IRQ4 | I | GPIO1_TSRL[2:3]=0b11<br>GPIO1_ISR3L[2:3]=0b01 |
| [IRQ5]GPIO38[UART0DTR][UART1Tx] | D32 | IRQ5 | I | GPIO1_TSRL[12:13]=0b11<br>GPIO1_ISR3L[12:13]=0b01 |
| [IRQ6]GPIO39[UART0RI][UART1Rx] | D34 | IRQ6 | I | GPIO1_TSRL[14:15]=0b11<br>GPIO1_ISR3L[14:15]=0b01 |
| [IRQ7]GPIO30[PerPar0][DMAReq2] | A20 | IRQ7 | I | GPIO0_TSRH[28:29]=0b11<br>GPIO0_ISR3H[28:29]=0b01 |
| [IRQ8]GPIO31[PerPar1][DMAAck2] | A16 | IRQ8 | I | GPIO0_TSRH[30:31]=0b11<br>GPIO0_ISR3H[30:31]=0b01 |
| [IRQ9]GPIO32[PerPar2][EOT2/TC2] | A14 | IRQ9 | I | GPIO1_TSRL[0:1]=0b11<br>GPIO1_ISR3L[0:1]=0b01 |
| [IRQ10]GPIO43[PerCS3][NFCE3][DMAReq1] | A22 | IRQ10 | I | GPIO1_TSRL[22:23]=0b11<br>GPIO1_ISR3L[22:23]=0b01 |

*Table 19. IRQ Signals*

| PPC460EX Signals | Ball | IRQ | I/O | Configuration |
|---|---|---|---|---|
| [IRQ11]GPIO44[PerCS4][DMAAck1] | E21 | IRQ11 | I | GPIO1_TSRL[24:25]=0b11<br>GPIO1_ISR3L[24:25]=0b01 |
| [IRQ12]GPIO45[PerCS5][EOT1/TC1] | D21 | IRQ12 | I | GPIO1_TSRL[26:27]=0b11<br>GPIO1_ISR3L[26:27]=0b01 |
| [IRQ13]GPIO46[PerAddr05][DMAReq0] | B32 | IRQ13 | I | GPIO1_TSRL[28:29]=0b11<br>GPIO1_ISR3L[28:29]=0b01 |
| [IRQ14]GPIO47[PerAddr06][DMAAck0] | C31 | IRQ14 | I | GPIO1_TSRL[30:31]=0b11<br>GPIO1_ISR3L[30:31]=0b01 |
| [IRQ15]GPIO48[PerAddr07][EOT0/TC0] | D30 | IRQ15 | I | GPIO1_TSRH[0:1]=0b11<br>GPIO1_ISR3H[0:1]=0b01 |

*Table 20. NAND Flash Controller (NDFC) Interface*

| PPC460EX Signals | Ball | NDFC | I/O | Configuration |
|---|---|---|---|---|
| [NFCE0]PerCS0 | E24 | NFCE0 | O | SDR0_CUST0[NCG0]=1<br>Use NFCE0 when booting directly from NAND flash.<br><br>When booting from NAND flash, use SLC NAND with Block 0 guaranteed. The guarantee on Block 0 means Block 0 does not contain any stuck bits. Block 0 even with the guarantee is still affected by soft errors.<br><br>Note: Software cannot check for ECC errors while executing code (IPL) directly from Block 0. |
| [NFCE1]GPIO41[PerCS1] | B22 | NFCE1 | O | SDR0_CUST0[NCG1]=1<br>GPIO1_OSRL[18:19]=0b01<br>GPIO1_TSRL[18:19]=0b01<br>Pull up required when used as a chip select. |
| [NFCE2]GPIO42[PerCS2] | D25 | NFCE2 | O | SDR0_CUST0[NCG2]=1<br>GPIO1_OSRL[20:21]=0b01<br>GPIO1_TSRL[20:21]=0b01<br>Pull up required when used as a chip select. |
| [NFCE3]GPIO43[PerCS3][DMAReq1][IRQ10] | A22 | NFCE3 | O | SDR0_CUST0[NCG3]=1<br>GPIO1_OSRL[22:23]=0b01<br>GPIO1_TSRL[22:23]=0b01<br>Pull up required when used as a chip select. |
| [NFALE]GPIO26 | A25 | NFALE | O | SDR0_CUST0[MEN]=0b10 |
| [NFCLE]GPIO25 | F26 | NFCLE | O | SDR0_CUST0[MEN]=0b10 |
| [NFRdyBusy]GPIO22 | C24 | NFRdyBusy | I | SDR0_CUST0[MEN]=0b10 |
| [NFREn]GPIO23 | B24 | NFREn | O | SDR0_CUST0[MEN]=0b10 |
| [NFWEn]GPIO24 | A24 | NFWEn | O | SDR0_CUST0[MEN]=0b10 |

*Table 20. NAND Flash Controller (NDFC) Interface*

| PPC460EX Signals | Ball | NDFC | I/O | Configuration |
|---|---|---|---|---|
| PerData00<br>PerData01<br>PerData02<br>PerData03<br>PerData04<br>PerData05<br>PerData06<br>PerData07<br>PerData08<br>PerData09<br>PerData10<br>PerData11<br>PerData12<br>PerData13<br>PerData14<br>PerData15 | C21<br>B21<br>A21<br>E20<br>D20<br>C20<br>D18<br>B20<br>E19<br>D19<br>E18<br>C19<br>A19<br>C18<br>B18<br>A18 | PerData00<br>PerData01<br>PerData02<br>PerData03<br>PerData04<br>PerData05<br>PerData06<br>PerData07<br>PerData08<br>PerData09<br>PerData10<br>PerData11<br>PerData12<br>PerData13<br>PerData14<br>PerData15 | I/O | The EBC and NDFC share the PerData signals. The function on these signals depends on which controller controls the interface.<br>For an 8-bit NAND Flash connect as follows:<br>  PerData00 <> NAND Flash data07<br>  PerData01 <> NAND Flash data06<br>  .<br>  .<br>  .<br>  PerData07 <> NAND Flash data00<br><br>For a 16-bit NAND Flash connect as follows:<br>  PerData00 <> NAND Flash data07<br>  PerData01 <> NAND Flash data06<br>  .<br>  .<br>  .<br>  PerData07 <> NAND Flash data00<br><br>  PerData15 <> NAND Flash data08<br>  PerData14 <> NAND Flash data09<br>  .<br>  .<br>  .<br>  PerData08 <> NAND Flash data15 |

*Table 21. PCIe*

| PPC460EX Signals | Ball | PCIe | I/O | Configuration |
|---|---|---|---|---|
| *PCI Express 0* | | | | |
| PCIE0AVReg[SATA0AVReg] | AA01 | PCIE0AVReg | na | Leave unconnected. |
| PCIE0RefClk[SATA0RefClk] | AA02 | PCIE0RefClk | I | PCIe reference clock, typically 100MHz<br>Must be AC coupled. |
| $\overline{\text{PCIE0RefClk}}$[$\overline{\text{SATA0RefClk}}$] | AA03 | $\overline{\text{PCIE0RefClk}}$ | I | |
| PCIE0CalRN[SATA0CalRN] | AB02 | PCIE0CalRN | na | External reference resistor. Attach a 1.37 kohm , 1% resistor between PCIE0CalRN and PCIE0CalRP to provide the reference for both the bias currents and the impedance calibration circuitry. |
| PCIE0CalRP[SATA0CalRP] | AB01 | PCIE0CalRP | na | |
| PCIE0Rx0[SATA0Rx0] | W04 | PCIE0Rx0 | I | |
| $\overline{\text{PCIE0Rx0}}$[$\overline{\text{SATA0Rx0}}$] | W05 | $\overline{\text{PCIE0Rx0}}$ | I | |
| PCIE0Tx0[SATA0Tx0] | W02 | PCIE0Tx0 | O | Output must be AC coupled |
| $\overline{\text{PCIE0Tx0}}$[$\overline{\text{SATA0Tx0}}$] | W01 | $\overline{\text{PCIE0Tx0}}$ | O | |
| *PCI Express 1* | | | | |

*Table 21. PCIe*

| PPC460EX Signals | Ball | PCIe | I/O | Configuration |
|---|---|---|---|---|
| PCIE1AVReg | R05 | PCIE1AVReg | na | Leave unconnected. |
| PCIE1RefClk | R04 | PCIE1RefClk | I | PCIe reference clock, typically 100MHz Must be AC coupled. |
| $\overline{\text{PCIE1RefClk}}$ | R03 | $\overline{\text{PCIE1RefClk}}$ | I | |
| PCIE1CalRN | P01 | PCIE1CalRN | na | External reference resistor. Attach a 1.37 kohm , 1% resistor between PCIE1CalRN and PCIE1CalRP to provide the reference for both the bias currents and the impedance calibration circuitry. |
| PCIE1CalRP | P02 | PCIE1CalRP | na | |
| PCIE1Rx0 | L05 | PCIE1Rx0 | I | |
| $\overline{\text{PCIE1Rx0}}$ | L04 | $\overline{\text{PCIE1Rx0}}$ | I | |
| PCIE1Rx1 | N05 | PCIE1Rx1 | I | |
| $\overline{\text{PCIE1Rx1}}$ | N04 | $\overline{\text{PCIE1Rx1}}$ | I | |
| PCIE1Rx2 | T04 | PCIE1Rx2 | I | |
| $\overline{\text{PCIE1Rx2}}$ | T05 | $\overline{\text{PCIE1Rx2}}$ | I | |
| PCIE1Rx3 | V05 | PCIE1Rx3 | I | |
| $\overline{\text{PCIE1Rx3}}$ | V04 | $\overline{\text{PCIE1Rx3}}$ | I | |
| PCIE1Tx0 | M02 | PCIE1Tx0 | O | Output must be AC coupled |
| $\overline{\text{PCIE1Tx0}}$ | M01 | $\overline{\text{PCIE1Tx0}}$ | O | |
| PCIE1Tx1 | N02 | PCIE1Tx1 | O | Output must be AC coupled |
| $\overline{\text{PCIE1Tx1}}$ | N01 | $\overline{\text{PCIE1Tx1}}$ | O | |
| PCIE1Tx2 | T02 | PCIE1Tx2 | O | Output must be AC coupled |
| $\overline{\text{PCIE1Tx2}}$ | T01 | $\overline{\text{PCIE1Tx2}}$ | O | |
| PCIE1Tx3 | V02 | PCIE1Tx3 | O | Output must be AC coupled |
| $\overline{\text{PCIE1Tx3}}$ | V01 | $\overline{\text{PCIE1Tx3}}$ | O | |

PCIe Port0 is selected during reset by bootstrap registers SDR0_SDSTP1[SATA ] and SDR0_PCF1[SATA].  Set SATA=0.

*Application Note*

*Table 22. PCI*

| PPC460EX Signals | Ball | PCI | I/O | Configuration |
|---|---|---|---|---|
| PCI0AD00 | D11 | PCI0AD00 | | |
| PCI0AD01 | E11 | PCI0AD01 | | |
| PCI0AD02 | B10 | PCI0AD02 | | |
| PCI0AD03 | A10 | PCI0AD03 | | |
| PCI0AD04 | C10 | PCI0AD04 | | |
| PCI0AD05 | F10 | PCI0AD05 | | |
| PCI0AD06 | D10 | PCI0AD06 | | |
| PCI0AD07 | A09 | PCI0AD07 | | |
| PCI0AD08 | D09 | PCI0AD08 | | |
| PCI0AD09 | A08 | PCI0AD09 | | |
| PCI0AD10 | F09 | PCI0AD10 | | |
| PCI0AD11 | B08 | PCI0AD11 | | |
| PCI0AD12 | C08 | PCI0AD12 | | |
| PCI0AD13 | D08 | PCI0AD13 | | |
| PCI0AD14 | A07 | PCI0AD14 | | |
| PCI0AD15 | F08 | PCI0AD15 | I/O | PCI0AD31 - MSb |
| PCI0AD16 | A05 | PCI0AD16 | | PCI0AD00 - LSb |
| PCI0AD17 | A04 | PCI0AD17 | | |
| PCI0AD18 | D05 | PCI0AD18 | | |
| PCI0AD19 | B04 | PCI0AD19 | | |
| PCI0AD20 | D02 | PCI0AD20 | | |
| PCI0AD21 | F04 | PCI0AD21 | | |
| PCI0AD22 | E03 | PCI0AD22 | | |
| PCI0AD23 | D03 | PCI0AD23 | | |
| PCI0AD24 | E01 | PCI0AD24 | | |
| PCI0AD25 | E04 | PCI0AD25 | | |
| PCI0AD26 | G05 | PCI0AD26 | | |
| PCI0AD27 | G04 | PCI0AD27 | | |
| PCI0AD28 | F02 | PCI0AD28 | | |
| PCI0AD29 | H06 | PCI0AD29 | | |
| PCI0AD30 | F01 | PCI0AD30 | | |
| PCI0AD31 | F05 | PCI0AD31 | | |
| PCI0C0/$\overline{BE0}$ | C09 | PCI0C/$\overline{BE0}$ | | |
| PCI0C1/$\overline{BE1}$ | C07 | PCI0C/$\overline{BE1}$ | I/O | |
| PCI0C2/$\overline{BE2}$ | C05 | PCI0C/$\overline{BE2}$ | | |
| PCI0C3/$\overline{BE3}$ | F03 | PCI0C/$\overline{BE3}$ | | |
| PCI0Clk | K01 | PCI0Clk | I | Typically 33MHz or 66MHz<br><br>Note: When the PCI interface is not used, drive this pin with a 3.3V clock signal at a frequency between 1 and 66MHz.<br><br>A clock must be present before reset. |
| $\overline{PCI0DevSel}$ | A06 | $\overline{PCI0DevSel}$ | I/O | 8.2Kohm pull-up required on host system. |
| $\overline{PCI0Frame}$ | E06 | $\overline{PCI0Frame}$ | I/O | 8.2Kohm pull-up required on host system. |
| $\overline{PCI0Gnt0}$/$\overline{Req}$ | G03 | $\overline{PCI0Gnt0}$/$\overline{Req}$ | O | |
| $\overline{PCI0Gnt1}$ | H04 | $\overline{PCI0Gnt1}$ | O | |
| $\overline{PCI0Gnt2}$ | G01 | $\overline{PCI0Gnt2}$ | O | |

*Application Note*

*Table 22. PCI*

| PPC460EX Signals | Ball | PCI | I/O | Configuration |
|---|---|---|---|---|
| PCI0Gnt3 | H03 | PCI0Gnt3 | O | |
| PCI0IDSel | D01 | PCI0IDSel | I | Connect PCI0IDSel to a PCI host via upper address pins, AD31:16. This signal is only used when the PPC460EX is used as a PCI adapter. A PCI adapter is any PCI device that is not the PCI Host. Only the PCI host initiates PCI configuration cycles.<br><br>When the PPC460EX is host, PCI0IDSel should be pull down. |
| PCI0Int | J04 | PCI0Int | O | PCI0Int is the PCI interrupt when the PPC460EX is a PCI adapter.<br><br>When the PPC460EX is the PCI host, connect PCI interrupt pins from the PCI adapters to IRQ input pins. |
| PCI0IRdy | C04 | PCI0IRdy | I/O | 8.2Kohm pull-up required on host system. |
| PCI0M66En | E09 | PCI0M66En | I | PCI0M66En is used when the PPC460EX is the PCI host to determine the highest supported bus frequency supported.<br><br>Pull down when the PPC460EX is a PCI adapter. |
| PCI0Par | D07 | PCI0Par | I/O | |
| PCI0PErr | B06 | PCI0PErr | I/O | 8.2Kohm pull-up required on host system. |
| PCI0Req0/Gnt | J06 | PCI0Req0/Gnt | I | Pull-up required when the PCI interface is used.<br><br>When the PCI interface is unused, disable the internal arbiter (SDR0_PCI0[PAE]=0) and pull PCI0Req0/Gnt down through a 1Kohm to ground. Driving Gnt low forces the PLB4 to PCI bridge to permanently park on the bus and drive PCIAD0:31 signals. |
| PCI0Req1 | H02 | PCI0Req1 | I | Pull-up required. |
| PCI0Req2 | K04 | PCI0Req2 | I | Pull-up required. |
| PCI0Req3 | J05 | PCI0Req3 | I | Pull-up required. |
| PCI0Reset | K03 | PCI0Reset | O | PCI0Reset is the reset output when the PPC460EX is the PCI host. This signal should only be used when the PPC460EX is the PCI Host.<br><br>Use SysReset as the reset input when the PPC460EX is a PCI adapter. |
| PCI0SErr | E07 | PCI0SErr | I/O | 8.2Kohm pull-up required on host system. |
| PCI0Stop | C06 | PCI0Stop | I/O | 8.2Kohm pull-up required on host system. |
| PCI0TRdy | D06 | PCI0TRdy | I/O | 8.2Kohm pull-up required on host system. |

When the PPC460EX is a PCI host, use  upper address pins, AD31:16 to select PCI adapters. Connect an upper address signal to the IDSel of each PCI adapter.

*Table 23. Reserved Signals Requiring Termination*

| Reserved Signals | Ball | Reserved | I/O | Configuration |
|---|---|---|---|---|
| Reserved | AM15 | Reserved | I | Pull-down using a 1kOhm to GND |
| Reserved | AN15 | Reserved | I | Pull-down using a 1kOhm to GND |

*Table 24. Reserved Signals Not Requiring Termination*

| Reserved Signals | Ball | Reserved | I/O | Configuration |
|---|---|---|---|---|
| Reserved | A17 | Reserved | - | Do not pull up or pull down. Leave unconnected. |
| Reserved | AL13 | Reserved | - | Do not pull up or pull down. Leave unconnected. |
| Reserved | AM13 | Reserved | - | Do not pull up or pull down. Leave unconnected. |
| Reserved | AL12 | Reserved | - | Do not pull up or pull down. Leave unconnected. |
| Reserved | AM12 | Reserved | - | Do not pull up or pull down. Leave unconnected. |
| Reserved | AP10 | Reserved | - | Do not pull up or pull down. Leave unconnected. |
| Reserved | AN10 | Reserved | - | Do not pull up or pull down. Leave unconnected. |

*Table 25. SATA Interface*

| PPC460EX Signals | Ball | SATA | I/O | Configuration |
|---|---|---|---|---|
| [SATA0AVReg]PCIE0AVReg | AA01 | SATA0AVReg | na | Leave unconnected. |
| [SATA0RefClk]PCIE0RefClk | AA02 | SATA0RefClk | I | SATA reference, 100MHz or 120MHz Must be AC coupled. |
| [SATA0RefClk]PCIE0RefClk | AA03 | SATA0RefClk | I | |
| [SATA0CalRN]PCIE0CalRN | AB02 | SATA0CalRN | na | External reference resistor. Attach a 1.37 kohm , 1% resistor between SATA0CalRNand SATA0CalRP to provide the reference for both the bias currents and the impedance calibration circuitry. |
| [SATA0CalRP]PCIE0CalRP | AB01 | SATA0CalRP | na | |
| [SATA0Rx0]PCIE0Rx0 | W04 | SATA0Rx0 | I | |
| [SATA0Rx0]PCIE0Rx0 | W05 | SATA0Rx0 | I | |
| [SATA0Tx0]PCIE0Tx0 | W02 | SATA0Tx0 | O | |
| [SATA0Tx0]PCIE0Tx0 | W01 | SATA0Tx0 | O | |

The SATA port is selected during reset by bootstrap registers SDR0_SDSTP1[SATA ] and SDR0_PCF1[SATA].  Set SATA=1.

*Table 26. SPI\* Interface*

| PPC460EX Signals | Ball | IIC1 | I/O | Configuration |
|---|---|---|---|---|
| SCPClkOut[IIC1SClk] | K31 | SCPClkOut | I/O | Set SDR0_PFC1[SIS]=0. |
| SCPDO[IIC1SData] | G34 | SCPDO | O | |
| SCPDI | K32 | SCPDI | I | |

\* A GPIO pins can be used to select SPI devices.

*Table 27. System Signals*

| PPC460EX Signals | Ball | System | I/O | Configuration |
|---|---|---|---|---|
| FSOURCE0 | E17 | FSOURCE0 | I | Manufacturing test signal (Reserved)<br><br>Must be pulled down. This signal can be connected directly to ground. A pull down resistor is not needed. If this signal is floats, the electronic chip id registers (SDR0_ECID0:3) may not respond with the correct ID when read. |
| $\overline{\text{HISRRset}}$ | B11 | $\overline{\text{HISRRset}}$ | I | HISRRST is a warm reset that when asserted, places the DDR memory in self-refresh and resets the PPC460EX. To place memory in self-refresh, assert HISRRST without asserting SysReset.<br><br>Pull-up is required. |
| SysClk | AD02 | SysClk | I | System Clock: 66.66MHz to 100MHz |
| SysErr | AB03 | SysErr | O | |
| $\overline{\text{SysReset}}$ | AC02 | $\overline{\text{SysReset}}$ | I | SysReset must be driven low for at least 32 SysClk Cycles in order to generate a reset. |
| TestEn | K29 | TestEn | I | Manufacturing test signal (Reserved)<br>Has internal pull down. |
| TherMonA | AM09 | TherMonA | na | |
| TherMonB | AL10 | TherMonB | na | |
| TmrClk | C11 | TmrClk | I | Set CCR1[TCS]=1 to select TmrClk as the clock source for the PPC440 CPU timer.<br><br>When CCR1[TCS]=0, the internal CPUClk is the PPC440 CPU timer source.<br><br>Has internal pull-up. |

*Table 27. System Signals*

| PPC460EX Signals | Ball | System | I/O | Configuration |
|---|---|---|---|---|
| [UART0CTS]GPIO36[DMAAck3][UART3Rx] | E31 | - | I | Ball E31, E34 and E32 are boot strap signals used to select the boot option. These signals are sampled on the rising edge of SysClk and latched on the first rising edge of SysClk after SysReset deasserts (driven high). |
| [UART0DCD]GPIO34[UART1CTS][UART2Tx] | E34 | - | I | |
| [UART0DSR]GPIO35[UART1RTS][UART2Rx] | E32 | - | I | |

*Table 28. UART0 8-pin mode*

| PPC460EX Signals | Ball | UART* | I/O | Configuration |
|---|---|---|---|---|
| [UART0CTS]GPIO36[DMAAck3][UART3Rx] | E31 | UART0_CTS | I | GPIO1_TSRL[8:9]=0b01<br>GPIO1_ISR1L[8:9]=0b01 |
| [UART0RTS]GPIO37[EOT3/TC3][UART3Tx] | D33 | UART0_RTS | O | GPIO1_OSRL[10:11]=0b01<br>GPIO1_TSRL[10:11]=0b01 |
| UART0_Rx | C34 | UART0_Rx | I | |
| UART0_Tx | C33 | UART0_Tx | O | |
| [UART0DCD]GPIO34[UART1CTS][UART2Tx] | E34 | UART0_DCD | I | GPIO1_TSRL[4:5]=0b01<br>GPIO1_ISR1L[4:5]=0b01 |
| [UART0DSR]GPIO35[UART1RTS][UART2Rx] | E32 | UART0_DSR | I | GPIO1_TSRL[6:7]=0b01<br>GPIO1_ISR1L[6:7]=0b01 |
| [UART0DTR]GPIO38[UART1Tx][IRQ5] | D32 | UART0_DTR | O | GPIO1_OSRL[12:13]=0b01<br>GPIO1_TSRL[12:13]=0b01 |
| [UART0RI]GPIO39[UART1Rx][IRQ6] | D34 | UART0_RI | I | GPIO1_TSRL[14:15]=0b01<br>GPIO1_ISR1L[14:15]=0b01 |

*Table 29. UART0 4-pin mode and UART1 4-pin mode*

| PPC460EX Signals | Ball | UART | I/O | Configuration |
|---|---|---|---|---|
| *UART0* | | | | |
| [UART0CTS]GPIO36[DMAAck3][UART3Rx] | E31 | UART0_CTS | I | GPIO1_TSRL[8:9]=0b01<br>GPIO1_ISR1L[8:9]=0b01<br><br>Set SDR0_PFC1[U0ME]=1 for UART0_CTS. |
| [UART0RTS]GPIO37[EOT3/TC3][UART3Tx] | D33 | UART0_RTS | O | GPIO1_OSRL[10:11]=0b01<br>GPIO1_TSRL[10:11]=0b01<br><br>Set SDR0_PFC1[U0ME]=1 for UART0_RTS. |
| UART0_Rx | C34 | UART0_Rx | I | |
| UART0_Tx | C33 | UART0_Tx | O | |
| *UART1* | | | | |
| [UART0DCD]GPIO34[UART1CTS][UART2Tx] | E34 | UART1_CTS | I | GPIO1_TSRL[4:5]=0b10<br>GPIO1_ISR2L[4:5]=0b01<br><br>Set SDR0_PFC1[U1ME]=1 for UART1_CTS. |
| [UART0DSR]GPIO35[UART1RTS][UART2Rx] | E32 | UART1_RTS | O | GPIO1_OSRL[6:7]=0b10<br>GPIO1_TSRL[6:7]=0b10<br><br>Set SDR0_PFC1[U1ME]=1 for UART1_RTS. |
| [UART0RI]GPIO39[UART1Rx][IRQ6] | D34 | UART1_Rx | I | GPIO1_TSRL[14:15]=0b10<br>GPIO1_ISR2L[14:15]=0b01 |
| [UART0DTR]GPIO38[UART1Tx][IRQ5] | D32 | UART1_Tx | O | GPIO1_OSRL[12:13]=0b10<br>GPIO1_TSRL[12:13]=0b10 |

*Table 30. UART0 4-pin mode, UART1 2-pin mode and UART2 2-pin mode*

| PPC460EX Signals | Ball | UART | I/O | Configuration |
|---|---|---|---|---|
| *UART0* | | | | |
| [UART0CTS]GPIO36[DMAAck3][UART3Rx] | E31 | UART0_CTS | I | GPIO1_TSRL[8:9]=0b01<br>GPIO1_ISR1L[8:9]=0b01<br><br>Set SDR0_PFC1[U0ME]=1 for UART0_CTS. |
| [UART0RTS]GPIO37[EOT3/TC3][UART3Tx] | D33 | UART0_RTS | O | GPIO1_OSRL[10:11]=0b01<br>GPIO1_TSRL[10:11]=0b01<br><br>Set SDR0_PFC1[U0ME]=1 for UART0_RTS. |
| UART0_Rx | C34 | UART0_Rx | I | |
| UART0_Tx | C33 | UART0_Tx | O | |
| *UART1* | | | | |
| [UART0RI]GPIO39[UART1Rx][IRQ6] | D34 | UART1_Rx | I | GPIO1_TSRL[14:15]=0b10<br>GPIO1_ISR2L[14:15]=0b01 |
| [UART0DTR]GPIO38[UART1Tx][IRQ5] | D32 | UART1_Tx | O | GPIO1_OSRL[12:13]=0b10<br>GPIO1_TSRL[12:13]=0b10 |
| *UART2* | | | | |
| [UART2Rx][UART0DSR]GPIO35[UART1RTS] | E32 | UART2Rx | I | GPIO1_TSRL[6:7]=0b11<br>GPIO1_ISR3L[6:7]=0b01 |
| [UART2Tx][UART0DCD]GPIO34[UART1CTS] | E34 | UART2Tx | O | GPIO1_OSRL[4:5]=0b11<br>GPIO1_TSRL[4:5]=0b11 |

*Table 31. UART0 2-pin mode, UART1 2-pin mode, UART2 2-pin mode and UART3 2-pin mode*

| PPC460EX Signals | Ball | UART | I/O | Configuration |
|---|---|---|---|---|
| *UART0* | | | | |
| UART0_Rx | C34 | UART0_Rx | I | |
| UART0_Tx | C33 | UART0_Tx | O | |
| *UART1* | | | | |
| [UART0RI]GPIO39[UART1Rx][IRQ6] | D34 | UART1_Rx | I | GPIO1_TSRL[14:15]=0b10<br>GPIO1_ISR2L[14:15]=0b01 |
| [UART0DTR]GPIO38[UART1Tx][IRQ5] | D32 | UART1_Tx | O | GPIO1_OSRL[12:13]=0b10<br>GPIO1_TSRL[12:13]=0b10 |
| *UART2* | | | | |
| [UART2Rx][UART0DSR]GPIO35[UART1RTS] | E32 | UART2Rx | I | GPIO1_TSRL[6:7]=0b11<br>GPIO1_ISR3L[6:7]=0b01 |
| [UART2Tx][UART0DCD]GPIO34[UART1CTS] | E34 | UART2Tx | O | GPIO1_OSRL[4:5]=0b11<br>GPIO1_TSRL[4:5]=0b11 |
| *UART3* | | | | |
| [UART3Rx][UART0CTS]GPIO36[DMAAck3] | E31 | UART3Rx | I | GPIO1_TSRL[8:9]=0b11<br>GPIO1_ISR3L[8:9]=0b01 |
| [UART3Tx][UART0RTS]GPIO37[EOT3/TC3] | D33 | UART3Tx | O | GPIO1_OSRL[10:11]=0b11<br>GPIO1_TSRL[10:11]=0b11 |

*Table 32. UARTSerClk Signal*

| PPC460EX Signals | Ball | UART | I/O | Configuration |
|---|---|---|---|---|
| UARTSerClk[LeakTest] | G30 | UARTSerClk | I | To select UARTSerClk as the Serial Clock set SDR0_UART0[U0EC]=1, for UART0 set SDR0_UART1[U1EC]=1, for UART1 set SDR0_UART2[U2EC]=1, for UART2 Set SDR0_UART3[U3EC]=1, for UART3 |
| | | | | The Serial Clock input to a UART is either UARTSerClk or the internal PLB Clk. Typically, the clock input for UARTSerClk is 11.0592MHz since this frequency generates the common baud rates.<br><br>Example:<br>9600 Baud<br>UARTSerClk = SerialClk = 11.059MHz<br>UARTDivisor=UARTx_DLM \| UARTx_DLL<br>BAUDRate=SerialClk/(16*UARTDivisor)=<br>11059200Hz/(16*72) = 9600 Baud<br><br>115200 Baud<br>UARTDivisor=UARTx_DLM \| UARTx_DLL<br>BAUDRate=SerialClk/(16*UARTDivisor)=<br>11059200Hz/(16*6) = 115200 Baud |
| | | | | When the PLB Clk is used as the Serial Clock source, the following applies:<br>SDR0_UARTn[Un1CS]=0010<br>SDR0_UARTn[UnEC]=0<br><br>SerialClock = PLBClk/SDR0_UARTn[UnDIV]<br>UARTDivisor=UARTx_DLM \| UARTx_DLL<br>BAUDRate=SerialClock/(16*UARTDivisor)<br><br>Example:<br>PLB=200MHz<br>9600 Baud<br>Serial Clock = PLBClk/SDR0_UARTn[UnDIV]=<br>200MHz/18=11.111MHz<br>BAUDRate=SerialClock/(16*UARTDivisor)=<br>11.111E6 Hz/(16*72)=9645.06Baud<br>100*(9645.06 -9600)/9600 = 0.47% error<br><br>115200 Baud<br>Serial Clock = PLBClk/SDR0_UARTn[UnDIV]=<br>200MHz/18=11.111MHz<br>BAUDRate=SerialClock/(16*UARTDivisor)=<br>1.111E6 Hz/(16*6)=115740.74 Baud<br>100*(115740.74 -115200)/115200 = 0.49% error |

*Table 33. ULPI USB 2.0 OTG Interface*

| PPC460EX Signals | Ball | USB | I/O | Configuration |
|---|---|---|---|---|
| USB2DClk | AF06 | USB2Clk | I | 60MHz |
| [USB2DD0]GPIO08<br>[USB2DD1]GPIO09<br>[USB2DD2]GPIO10<br>[USB2DD3]GPIO11<br>[USB2DD4]GPIO12<br>[USB2DD5]GPIO13<br>[USB2DD6]GPIO14<br>[USB2DD7]GPIO15 | AH04<br>AJ05<br>AG06<br>AJ02<br>AJ04<br>AH03<br>AJ01<br>AH01 | USB2DD0<br>USB2DD1<br>USB2DD2<br>USB2DD3<br>USB2DD4<br>USB2DD5<br>USB2DD6<br>USB2DD7 | I/O | USB2DD7 - MSb<br>USB2DD0 - LSb<br><br>GPIO0_OSRL[16:31]=0x55<br>GPIO0_TSRL[16:31]=0x55<br>GPIO0_ISR1L[16:31]=0x55 |
| [USB2DDir]GPIO21 | AD04 | USB2DDir | I | GPIO0_TSRH[10:11]=0b01<br>GPIO0_ISR1H[10:11]=0b01 |
| [USB2DNext]GPIO20 | AG03 | USB2DNext | I | GPIO0_TSRH[8:9]=0b01<br>GPIO0_ISR1H[8:9]=0b01 |
| [USB2DStop]GPIO19 | AF03 | USB2DStop | O | GPIO0_OSRH[6:7]=0b01<br>GPIO0_TSRH[6:7]=0b01 |

*Table 34. ULPI USB 2.0 Host Interface*

| PPC460EX Signals | Ball | USB | I/O | Configuration |
|---|---|---|---|---|
| USB2HClk | AC06 | USB2HClk | I | 60MHz |
| USB2HClk48 | AE06 | USB2HClk48 | I | 48Mhz |
| [USB2HD0]GPIO00<br>[USB2HD1]GPIO01<br>[USB2HD2]GPIO02<br>[USB2HD3]GPIO03<br>[USB2HD4]GPIO04<br>[USB2HD5]GPIO05<br>[USB2HD6]GPIO06<br>[USB2HD7]GPIO07 | AG01<br>AD05<br>AE04<br>AF01<br>AE02<br>AE01<br>AB05<br>AD03 | USB2HD0<br>USB2HD1<br>USB2HD2<br>USB2HD3<br>USB2HD4<br>USB2HD5<br>USB2HD6<br>USB2HD7 | I/O | USB2HD7 - MSb<br>USB2HD0 - LSb<br><br>GPIO0_OSRL[0:15]=0x55<br>GPIO0_TSRL[0:15]=0x55<br>GPIO0_ISR1L[0:15]=0x55 |
| [USB2HDir]GPIO18 | AG04 | USB2HDir | I | GPIO0_TSRH[4:5]=0b01<br>GPIO0_ISR1H[4:5]=0b01 |
| [USB2HNext]GPIO17 | AG02 | USB2HNext | I | GPIO0_TSRH[2:3]=0b01<br>GPIO0_ISR1H[2:3]=0b01 |
| [USB2HStop]GPIO16 | AF04 | USB2HStop | O | GPIO0_OSRH[0:1]=0b01<br>GPIO0_TSRH[0:1]=0b01 |

## Revision Log

| Date | Version | Contents of Modification |
|---|---|---|
| 12/13/2007 | 0.00 | • Reviewed signal names against engineering spreadsheet and the 460EX data sheet |
| 02/26/2008 | 0.01 | • Updated GPIO settings<br>• Added a recommendation for HISRRST |
| 02/27/2008 | 0.02 | • Added SDR0_PFC1 settings to the UART description. |
| 02/27/2008 | 0.03 | • Corrected the description of the DDR Clock Enable signal.<br>• Corrected typos in the UART settings (SDR0_PFC1[U0ME] and SDR0_PFC1[U1ME]). |
| 03/13/2008 | 1.00 | • Corrected GPIO registers settings for USB signals in Tables 29 and 30.<br>• Added recommendation for SGMII0RxClk and SGMII1RxClk signals in Table 12.<br>• Removed requirement for GMC0_RefClk in MII mode.<br>• Added register settings for Ethernet modes to Tables 8-13. |
| 03/18/2008 | 1.01 | • Replaced Advanced with Preliminary. The document has been reviewed by development.<br>• Removed IRQ0:3 from Figure 1. IRQ0:3 are shared with GPIO signals only.<br>• Correction in Table 5. TDI, TMS, TRST and HALT have internal pull-ups.<br>• Corrected GPIO register names in Table 6.<br>• Removed GPIO1_ISR1L and GPIO1_ISR1H settings for PerAddr5:7 in Table 7.<br>• Corrected typo with SDR0_ETH_CFG register name in Tables 8, 9, 10 and 11.<br>• Replaced SDR0_ETH_CFG[GMC0_BRISDGE_SEL] with SDR0_ETH_CFG[GMC0BS].<br>• Removed GPIO settings from Table 18. The NDFC is mux'ed with the GPIO between the GPIO controller and the I/O. No GPIO register settings required to use the NDFC.<br>• Corrected GPIO setting for UART0_RTS in Table 28.<br>• Corrected GPIO setting for UART2Tx in Table 29.<br>• Corrected GPIO register names in Tables 29 and 30. |
| 03/18/2008 | 1.02 | • Added DMA2P40_CRn[ETD] bit field settings for EOT/TC signals in Table 6.<br>• Removed note about required pull-up for TmrClk in Table 23.<br>• Updated settings for UART 4 pin mode in Table 29 and Table 30. RTS/CTS signaling should be used in 4-pin mode.<br>• Removed SGMIIRefClk and SGMIIRefClk from Table 12. Use of the differential SGMIIRef-Clk is not recommended. The single ended 125MHz GMCRefClk should be used in place of SGMIIRefClk. |
| 04/15/2008 | 1.03 | • Removed reset requirement for HISRRST in Table 23. HISRRST should be pulled up during a power on reset. There are no requirements for driving this signal low during a power on reset. HISRRST is used only when it is needed to place the DDR memory in self refresh during a warm reset.<br>• Added the following requirement for SysReset in Table 23: SysReset must be driven low for at least 32 SysClk cycles in order to generate a reset. |
| 05/08/2008 | 1.04 | • Corrected MSb and LSb for DDR data signals in Table 3. MemData00 is the MSb and MemData63 is the LSb.<br>• Added comments on how MemAddr signals should be connected in Table 3.<br>• Corrected the TrcClk frequency in Table 4. The PPC440 processor TrcClk operates at 1/4 the CPU Clk frequency. |
| 08/06/2008 | 1.05 | • Corrected NAND flash interface recommendation for 16 bit NAND flash in Table 18.<br>• Removed references to the DC bias on PCIe RX signals in Table 19. |

| Date | Version | Contents of Modification |
|---|---|---|
| 10/27/2008 | 1.06 | • Removed references to SMII and RMII.<br>• Added comments about biasing and termination of SGMII signals in *Table 15*.<br>• Moved the Ethernet and UART interface configuration descriptions to *Table 1* - 4 and 6.<br>• Added foot note to DMA signal table, *Table 10*. Check errata before using DMA.<br>• Added foot note toSGMII signal table, *Table 15*. Check errata before using SGMII.<br>• Added comment to *Figure 1* indicating that PCIE0 is the 1 lane PCIe port.<br>• Corrected typo affecting GPIO25 and GPIO26 signal names in the GPIO column of *Table 16*.<br>• Added GMC0TxClk to the GMII Signal Configuration *Table 13*.<br>• Added *Table 23* to highlight reserved signals requiring termination.<br>• Corrected typo affecting TrcTS6 in the Trace column of *Table 8*.<br>• Removed comment stating that SysReset is an output in *Table 22*. SysReset is an input only. When the 460EX is used as a PCI adapter, a buffer is not required to prevent SysReset from driving the Host's PCIReset.<br>• Added a comment to the PCIClk Configuration column in Table 22. A clock is required for PCIClk, when the PCI interface is not used. |
| 11/03/2008 | 1.07 | • Replaced "GMC0TxEn, GMC1TxCtl "with "GMC0TxEn, GMC0TxCtl". This change affects Table 12 and Table 13.<br>• Removed square brackets from around SPI signals and placed them around IIC1 signals. This change affected Table 26..<br>• Replaced PCIC/BE0, PCIC/BE1, PCIC/BE2, PCIC/BE3 with PCIC0/BE0, PCIC1/BE1, PCIC2/BE2, PCIC3/BE3 in Table 22. |
| 12/11/2008 | 1.08 | • Added a statement to the Ethernet MDIO signals indicating the MDIO interface must be accessed through the EMAC0_STACR register. Due to erratum EMAC_3, EMAC1_STACR should not be used when accessing an external PHY. SDR0_ETH_CFG[MDIO_SEL]=00 is the only valid setting.<br>• Added additional information to the termination recommendation for PCI0Req0/Gnt. |
| 02/09/2009 | 1.09 | • Corrected SCPDI and SCPDO I/O type in Table 26. |
| 02/25/2009 | 1.10 | • Added "Duplicate clocks enables" to the ClkEn0:3 configuration comments in Table 7.<br>• Added "Connect to the same reference" to the MemVRef1A, MemVRef1B, MemVRef2A and MemVRef2B configuration comments in Table 7.<br>• Deleted "SDR0_CUST0[NCG3]=0" from Table 11 for PerCS4.<br>• Deleted "SDR0_CUST0[NCG3]=0" from Table 11 for PerCS5.<br>• Added GPIO register configurations to Table 20 for NFCE1, NFCE2 and NFCE3. |
| 06/17/2009 | 1.11 | • Added "Must be AC coupled" to [SATA0RefClk]PCIE0RefClk/[SATA0RefClk]PCIE0RefClk and PCIE1RefClk/[PCIE1RefClk description.<br>• Updated description of SGMII receiver and transmitter termination in Table 15.<br>• Added FSOURCE0, TestEn and bootstrap signals to Table 27.<br>• Added comments about PerCS0 and NFCE0 signals.<br>• Added Table 24, *Reserved Signals Not Requiring Termination* |
| 11/16/2009 | 1.12 | • Corrected comment for DDR ClkEn signals. Clock enables are assigned by rank. ClkEn0 is used by Rank0, ClkEn1 is used by Rank1, etc. |
| 02/05/2010 | 1.13 | • Change to GMC0RxClk in Table 14. GMC0RxClk required by EMAC0 and EMAC1. |

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