

Config. program ☒ V1.01
Firmware for BDI2000 ☒ V1.01
Logic for BDI2000 ☐ V1.06

ABATRON

Date: January 6, 2006

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Enhancements

- Telnet history buffer no longer filled with repeated commands.
- The Windows setup tools now allows to select a COM port in the range 1 - 19.
- The Telnet CONFIG command displays the firmware version.

Error Correction

- Correct single step of the Thumb BX pc instruction.
- Correct handling of ARM/Thumb mode switch while in debug state.

Config. program ☐ V1.01
Firmware for BDI2000 ☒ V1.02
Logic for BDI2000 ☐ V1.06

ABATRON

Date: June 9, 2006

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Enhancements

- Enhanced flash erase support via configuration file (see user's manual).
- Improved Telnet history buffer handling.
- Support for low level scan chain configuration added (see user's manual).

Error Correction

- Correct display of banked registers (rdall command).

Config. program ☐ V1.01
Firmware for BDI2000 ☒ V1.03
Logic for BDI2000 ☐ V1.06

ABATRON

Date: June 22, 2007

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Enhancements

- New flash algorithm types added (S29M64X8, S29M32X16).
- The MirrorBit algorithm uses the write buffer also when no workspace is defined.
- New RECONNECT option to the DEBUGPORT parameter added. When present, a Telnet/GDB (TCP) connection request to an already open TCP channel is accepted if the host IP is the same as the initial one. The old TCP channel will be closed immediately.
- Telnet accepts now multiple commands separated by a semi-colon on one line.

Config. program ☒ V1.02
Firmware for BDI2000 ☒ V1.04
Logic for BDI2000 ☐ V1.06

ABATRON

Date: Oct 28, 2007

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Enhancements

- Support for Cortex-A8 (OMAP3430) added.

Config. program ☐ V1.02
Firmware for BDI2000 ☒ V1.05
Logic for BDI2000 ☐ V1.06

ABATRON

Date: January 3, 2008
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Enhancements

- The new CLOCK init list entry allows to change the JTAG clock frequency during processing of the init list. Maybe useful to switch to a faster clock as soon as possible.
- Improved memory access for Cortex-A8
- Improved OMAP3430 reset sequence.

Error Correction

- Error in I28BX16 target programming algorithm corrected. Programming with workspace was very slow because the algorithm did not enter debug mode after terminating.
- ARM11: The displayed cache TAG values are now correct.
- Cortex-A8: The RESET signal is now released at the end of the standard reset sequence.

Config. program ☐ V1.02
Firmware for BDI2000 ☒ V1.06
Logic for BDI2000 ☐ V1.06

ABATRON

Date: April 10, 2008

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Error Correction

- Cortex-A8: Correct fast/stalled memory access sequences.

Config. program ☐ V1.02
Firmware for BDI2000 ☒ V1.07
Logic for BDI2000 ☐ V1.06

ABATRON

Date: July 9, 2008

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Enhancements

- Support for ARM1176 and Cortex-M3 (STM32) added.
- Support for STM32F10xx internal flash programming added.

Config. program ☐ V1.02
Firmware for BDI2000 ☒ V1.08
Logic for BDI2000 ☐ V1.06 / 1.00

ABATRON

Date: Aug. 29, 2008

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Enhancements

- Support for Luminary Micro Stellaris LM3S internal flash programming added.
- Support for Cortex-M3 / Cortex-A8 Single Wire Debug Mode added (different firmware).

Config. program ☐ V1.02
Firmware for BDI2000 ☒ V1.09
Logic for BDI2000 ☐ V1.06 / 1.00

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Date: Febr. 25, 2009

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Enhancements

- Support for Cortex-R4 added
- Support for ARM7 connected via JTAG-AP added (see manual).
- New parameter to select the single step mode added (see manual).
- New Telnet commands INTENA and INTDIS added.

Error Correction

- Correct single step of newer ARMv6/v7 instructions.

Config. program ☐ V1.02
Firmware for BDI2000 ☒ V1.10
Logic for BDI2000 ☐ V1.06 / 1.00

ABATRON

Date: Sept. 29, 2009

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Enhancements

- Support for DAP-Lite module added.
- Support for multiple A8/A9 debug components behind one DAP added.
- Support for searching nested ROM tables added.
- APB base address of the debug component can be preset (no ROM table search).
- Download speed via GDB improved.
- Support for a different reset type for the initial power-up reset added (see manual).

Config. program ☐ V1.02
Firmware for BDI2000 ☒ V1.11
Logic for BDI2000 ☒ V1.06 / 1.01

ABATRON

Date: May 17, 2010

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Enhancements

- Support for Atmel SAM3U / SAM3S internal flash programming added.
- SWD: Single Wire Output can be routed to a TCP/IP channel (see manual).

Config. program ☐ V1.02
Firmware for BDI2000 ☒ V1.12
Logic for BDI2000 ☐ V1.06 / 1.01

ABATRON

Date: August 20, 2010

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Enhancements

- Support for Cortex-M0 added.
- Support for LPC1xxx flash programming added.

Config. program ☐ V1.02
Firmware for BDI2000 ☒ V1.13
Logic for BDI2000 ☐ V1.06 / 1.01

ABATRON

Date: Dec. 23, 2010

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Enhancements

- Support for STM32L15 internal flash programming added.
- Support for EFM32 internal flash programming added.
- A8: Correct handling of synchronous watchpoints (step over during a restart).
- Get actual number of implemented break/watch points from DIDR register.

Error Correction

- M3: Correct sequence to set debug control bits (e.g. C_MASKINTS) before resume.
- A8/R4: Correct sequence to set PC before resume (use mov pc,r0 instead of bx r0).

Config. program ☐ V1.02
Firmware for BDI2000 ☒ V1.14
Logic for BDI2000 ☐ V1.06 / 1.01

ABATRON

Date: April 1, 2011
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Enhancements

- Support for Cortex-M4 added.
- Support for Freescale Kinetis internal flash programming added.
- New EXEC init list entry added (see manual).
- Special DAPPC configuration parameter added for TI processors (see manual).
- New Telnet MMU command allows to disable / enable the MMU.
- New PMM (Physical Memory Mapped) register type accesses memory always with disabled MMU.
- The BDI no longer automatically steps over a GDB set breakpoint at the current PC. This allows to use the GDB „jump“ command.

Error Correction

- A8/R4: Correct setting of instruction HWBP (Byte Select in BCR) for Thumb / Big Endian code.

Config. program ☐ V1.02
Firmware for BDI2000 ☒ V1.15
Logic for BDI2000 ☐ V1.06 / 1.01

ABATRON

Date: Nov. 29, 2011

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Enhancements

- Support for STM32F2 and STM32F4 internal flash programming added.

Config. program ☐ V1.02
Firmware for BDI2000 ☒ V1.16
Logic for BDI2000 ☐ V1.06 / 1.01

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Date: June 22, 2012

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Enhancements

- New startup mode „idle“ added. An idle core will not be accesses until attached via Telnet.
- New Telnet command „state“ shows the state of all cores.
- New Telnet commands „attach“ and „detach“ added.
- New SCANINIT command „m“ allows to write to AHB memory space.
- Support for Spansion S29VS-R flash added (S29VSRX16 algorithm)
- The JTAG clock frequency can be entered in Hertz and not only as an index.
- GDB: The BDI now answers with 1 to the GDB qAttached packet.

Config. program ☐ V1.02 / 1.00
Firmware for BDI2000 ☒ V1.17
Logic for BDI2000 ☒ V1.07 / 1.01

ABATRON

Date: April 2, 2013
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Enhancements

- Support for STM32W internal flash added.
- Support for STM32F10 dual bank flash (XL-density) added.
- Maximal Telnet and GDB remote command length increased to 256 characters.
- Telnet command UPDATE added that allows to reload the configuration file without booting the BDI.
- The reset pin is no longer observed when reset mode NONE is defined.
- The Telnet commands attach and detach accept a core number as parameter.
- Kinetis: FSEC is programmed to unsecure also after a chip erase.
- Kinetis: Programming FSEC to a secure state is refused.
- Kinetis: Info about how to unsecure a secured device added (see kinetis_unsecure.cfg).
- Accept APB debug base addresses below 0x80000000 in order to support BCM5301x.
- Telnet access to FP registers for Cortex-A and Cortex-R added (rdfp and rmfp command).
- Support for Cortex-A5, Cortex-A7 and Cortex-A15 added.
- Cortex-A: Clear OS Lock Access bit after target power-up.
- Support for Cortex-M external flash programming with workspace added (Thumb algorithm).
Output an error for not supported Flash/Buswidth combinations instead of simply loading the ARM algorithm.
- Support for simple bit manipulation (read/modify/write) via init list added. The RMx entry defines the address, the size and an optional XOR pattern.

```
RM8  <address> [<xor>]
RM16 <address> [<xor>]
RM32 <address> [<xor>]
WMX  <and> <or>
```

Example:

```
RM32 0x20000000 0x10101010 ;read and XOR
WMX  0xff00ff00 0x00000003 ;AND, OR and write back
```

- Init list entry added that waits until memory becomes a defined value. The RMx entry defines the address and the size for the following WAIT.

```
RM8  <address>
RM16 <address>
RM32 <address>
WAIT <mask> <equal>
```

Example:

```
RM16 0x2000000a ;define address and size
WAIT 0x0000f0ff 0x00001034 ;wait until ((value & mask) == equal)
```

Config. program ☐ V1.02 / 1.00
Firmware for BDI2000 ☒ V1.18
Logic for BDI2000 ☐ V1.07 / 1.01

ABATRON

Date: August 9, 2013
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Enhancements

- Support for STM32F0 internal flash added.
- Support for Kintetis FTFE and FTFA internal flash added.
- The WREG init list entry now accepts all names from the register definition file.
- Telnet access to 64-bit CPxx registers added (see user's manual).
- New Telnet command MODE allows to switch current processor mode.
- Cortex-A: New Telnet commands SECURE and NONSECURE allows to switch secure state.
- Cortex-M: AHB access port select parameter added. Used for Vybrid Cortex-M4 debug accesses.

Config. program ☒ V1.02
Firmware for BDI2000 ☒ V1.19
Logic for BDI2000 ☐ V1.07 / 1.01

ABATRON

Date: March 5, 2014

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Enhancements

- Support for ARM BE8 big endian mode added.
- Cortex-A: Improved core halted detection.
- Cortex-A: A new configuration parameter enables CTI support and defines the APB base address of the CTI component. It also defines the core group used when GDB sends the "continue" command.
- New and changed Multi-Core related Telnet commands.
- Configuration and register definitions can be stored in the BDI internal Flash memory. In this case no TFTP server is necessary to load the configuration files.

Config. program ☐ V1.02
Firmware for BDI2000 ☒ V1.20
Logic for BDI2000 ☐ V1.07 / 1.01

ABATRON

Date: May 30, 2014
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Enhancements

- The BREAKMODE configuration parameter allows to set the break/watch control bits SSC, HMC and PMC in DBGBCR and DBGWCR:

BREAKMODE {SOFT | HARD} [{HYP | <control>}]

HYP adds the hypervisor mode bit to the control value

<control> defines the SSC, HMC and PMC bits in DBGBCR and DBGWCR

Default is SSC=00, HMC=0 and PMC=11 (0x00000006)

Examples:

BREAKMODE SOFT	;control = 0x00000006
BREAKMODE HARD	;control = 0x00000006
BREAKMODE HARD HYP	;control = 0x00002006
BREAKMODE HARD 0x00002006	;control = 0x00002006

- New Telnet QUERY command to display parts of the configuration.

QUERY [<core>]

Examples:

BDI> query	displays common and core specific configuration for all cores
BDI> query 1	displays the core specific configuration of the selected core

Error Correction

- The CTI registers of not attached cores are no longer accessed during multi-core restart.

Config. program ☐ V1.02
Firmware for BDI2000 ☒ V1.21
Logic for BDI2000 ☐ V1.07 / 1.01

ABATRON

Date: Nov. 4, 2014
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Enhancements

- Support for Freescale LS1 (ARMv7, LS1021A, ...) added.
- SWAP option for register definitions added. Useful when accessing big endian registers from a little endian core or vice versa.
- A new configuration parameter option allows to define the protection bits for AHB/AXI accesses.
- For LS1, memory accesses via System Access Port (SAP) are supported.

Config. program ☐ V1.02
Firmware for BDI2000 ☒ V1.22
Logic for BDI2000 ☐ V1.07 / 1.01

ABATRON

Date: July 3, 2015

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Enhancements

- Core halted detection: Check only HALT bit in DSCR, ignore Monitor Debug Mode.
- Process init list entries for running cores if possible (memory access AHB/SAP).

Error Correction

- Cortex-R4: Correct handling of instruction big endian mode.
- Display correct STEPMODE in Telnet QUERY command.
- Display correct CPUTYPE in Telnet QUERY command for LS1000.
- Correct handling of core numbers > 9 (#nbr) in the configuration file.